The Telecommunications and Data Acquisition Progress Report 42-96

October–December 1988

E.C.Posner
Editor

February 15, 1989

National Aeronautics and
Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

The Telecommunications and Data Acquisition Progress Report 42-96

October–December 1988

E.C.Posner
Editor

February 15, 1989

National Aeronautics and
Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

The research described in this publication was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Preface

This quarterly publication provides archival reports on developments in programs managed by JPL's Office of Telecommunications and Data Acquisition (TDA). In space communications, radio navigation, radio science, and ground-based radio and radar astronomy, it reports on activities of the Deep Space Network (DSN) and its associated Ground Communications Facility (GCF) in planning, in supporting research and technology, in implementation, and in operations. Also included is TDA-funded activity at JPL on data and information systems and reimbursable DSN work performed for other space agencies through NASA. The preceding work is all performed for NASA's Office of Space Operations (OSO). The TDA Office also performs work funded by two other NASA program offices through and with the cooperation of the Office of Space Operations. These are the Orbital Debris Radar Program (with the Office of Space Station) and 21st Century Communication Studies (with the Office of Exploration).

In the search for extraterrestrial intelligence (SETI), the *TDA Progress Report* reports on implementation and operations for searching the microwave spectrum. In solar system radar, it reports on the uses of the Goldstone Solar System Radar for scientific exploration of the planets, their rings and satellites, asteroids, and comets. In radio astronomy, the areas of support include spectroscopy, very long baseline interferometry, and astrometry. These three programs are performed for NASA's Office of Space Science and Applications (OSSA), with support by the Office of Space Operations for the station support time.

Finally, tasks funded under the JPL Director's Discretionary Fund and the Caltech President's Fund which involve the TDA Office are included.

This and each succeeding issue of the *TDA Progress Report* will present material in some, but not necessarily all, of the following categories:

OSO Tasks:
- DSN Advanced Systems
  - Tracking and Ground-Based Navigation
  - Communications, Spacecraft-Ground
  - Station Control and System Technology
  - Network Data Processing and Productivity
- DSN Systems Implementation
  - Capabilities for Existing Projects
  - Capabilities for New Projects
  - New Initiatives
  - Network Upgrade and Sustaining
- DSN Operations
  - Network Operations and Operations Support
  - Mission Interface and Support
  - TDA Program Management and Analysis
- Communications Implementation and Operations
- Data and Information Systems
- Flight-Ground Advanced Engineering

OSO Cooperative Tasks:
- Orbital Debris Radar Program
- 21st Century Communication Studies

OSSA Tasks:
- Search for Extraterrestrial Intelligence
- Goldstone Solar System Radar
- Radio Astronomy

Discretionary Funded Tasks

Contents

OSO TASKS
DSN Advanced Systems
COMMUNICATIONS, SPACECRAFT-GROUND

Design and Test of a 2.25-MW Transformer Rectifier Assembly 1 S1
R. Cormier and J. Daeges
NASA Code 310-20-64-22-00

On Sampling Band-Pass Signals 14 S2
R. Sadr and M. Shahshahani
NASA Code 310-30-70-84-02

The Use of Interleaving for Reducing Radio Loss in Convolutionally Coded Systems 21 S3
D. Divsalar, M. K. Simon, and J. H. Yuen
NASA Code 310-30-71-83-04

A New VLSI Architecture for a Single-Chip-Type Reed-Solomon Decoder 40 S4
I. S. Hsu and T. K. Truong
NASA Code 310-30-71-87-02

A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes 49 S5
T. K. Truong, J. K. Holmes, I. S. Reed, and X. Yin
NASA Code 310-30-70-87-02

STATION CONTROL AND SYSTEM TECHNOLOGY

Test Aspects of the JPL Viterbi Decoder 59 S6
M. A. Breuer
NASA Code 310-30-72-88-01

On Testing VLSI Chips for the Big Viterbi Decoder 80 S7
I. S. Hsu
NASA Code 310-30-72-88-01

Wiring Viterbi Decoders (Splitting deBruijn Graphs) 93 S8
O. Collins, F. Pollara, S. Dolinar, and J. Statman
NASA Code 310-30-72-88-01

DSN Systems Implementation
CAPABILITIES FOR EXISTING PROJECTS

Block Diagrams of the Radar Interface and Control Unit 104 S9
J. W. Collier
NASA Code 314-40-41-91-92

CAPABILITIES FOR NEW PROJECTS

RF Performance Measurement of the DSS-14 70-Meter Antenna at C-Band/L-Band 117 S10
M. S. Gatti, A. J. Freiley, and D. Girdner
NASA Code 314-30-64-70-03

Microwave Time Delays for the Dual L-C-Band Feed System 126 S11
J. Chen
NASA Code 314-30-64-70-03

Systems Analysis for DSN Microwave Antenna Holography 132 S12
D. J. Rochblatt
NASA Code 314-30-50-70-01

DSN Operations
TDA PROGRAM MANAGEMENT AND ANALYSIS

Ka-Band Study—1988 ..... 158 S13
J. W. Layland, R. L. Horttor, R. C. Clauss, J. H. Wilcher,
R. J. Wallace, and D. J. Mudgway
NASA Code 314-40-31-30-03

Flight-Ground Advanced Engineering

A Low-Loss Linear Analog Phase Modulator for 8415 MHz Transponder Application 172 S14
N. Mysoor
NASA Code 315-91-10-12-02

OSSA Tasks
Search for Extraterrestrial Intelligence

Radio Frequency Interference Survey Over the 1.0 – 10.4 GHz Frequency Range at the Goldstone-Venus Development Station 179 S15
S. Gulkis, E. T. Olsen, M. J. Klein, and E. B. Jackson
NASA Code 314-30-69-08-32

Errata 189

Errata 191

Author Index, 1988 193

Design and Test of a 2.25-MW Transformer Rectifier Assembly

R. Cormier and J. Daeges
Radio Frequency and Antenna Microwave Subsystems Section

A new 2.25-MW transformer rectifier assembly has been fabricated for DSS-13 at Goldstone, California. The transformer rectifier will provide constant output power of 2.25 MW at any voltage from 31 kV to 125 kV. This will give a new capability of 1 MW of rf power at X-band, provided appropriate microwave tubes are in the power amplifier. A description of the design and test results is presented in this article.

I. Introduction

High-power transmitters are operational on the 70-meter antennas of the Deep Space Network. These transmitters provide uplink communication to the planetary satellites, and provide radar capability at DSS-14 to research the solar planets and their moons.

High-power transmitter microwave tubes presently used and those projected for the future are listed in Table 1. Note in particular the change in body current requirements from the early tubes, such as the X-3060, and those presently designed, such as VKS-7864. A decrease of nearly two orders of magnitude is seen. The importance of this is in the design of the klystron's protective circuits. The body current is monitored in the ground return to the power supply, and an increase of body current indicates beam heating of the klystron cavities, with potential damage unless the beam is removed. Unfortunately, ground currents from the transformer rectifier assembly cannot be separated from body currents. These currents from the transformer rectifier cause false operation of the protective circuits, especially in the newer tubes, where the maximum body current is now less than the ground currents from other sources. This has led to a need for tighter control on the ground currents in the transformer rectifier assembly.

The prime power for the transformer rectifier is obtained from a motor-generator set. This arrangement has the advantage of generating a regulated ac that can be adjusted to any voltage from practically zero to 2400 volts. The generator field is controlled from the output dc high voltage, forming a closed feedback loop. A regulation of 0.01 percent is maintained long term. Full power is obtained only from 2200 to 2400 volts. A frequency of 400 Hz is used to reduce the size of magnetic components. In addition, this allows wider regulator bandwidth. Table 2 summarizes the capabilities of each of the stations.

The new transformer rectifier assembly has the capability of powering all tubes presently used or proposed for future use. The size is 103-1/2 inches wide by 98-3/4 inches deep by 115-5/8 inches high. The total weight is approximately 60,000 pounds. The assembly is shown in Fig. 1.

II. Transformer

The transformer windings are mounted on a three-legged core type magnetic circuit. The windings consist of 12 identical coils, four mounted side by side on each leg. The primaries on each leg are connected in parallel and the three legs are connected in delta. The primaries have eight taps to provide a 2 to 1 range of output voltage. The secondaries are individually connected in extended delta to provide four three-phase outputs. Two of the deltas are phase shifted −15 degrees while the other two are phase shifted +15 degrees. In effect, the transformer converts the three-phase input to two six-phase outputs. Each secondary feeds a full-wave bridge rectifier that converts the ac to dc voltage. A schematic of the transformer rectifier is shown in Fig. 2.

The use of extended delta windings has the advantage of physical coil symmetry. This makes the manufacturing process easier due to winding of identical coils. Electrically, the advantages are identical output voltage values for each set of deltas and equal inductances in each phase, which reduce the uncharacteristic harmonics on both the ac and dc sides of the transformer rectifier assembly [1].

The results of measurements of the dc harmonics are shown in Fig. 3. For comparison purposes, a plot of the old unit is included as Fig. 4.

The use of taps on the primary for a voltage range of 2 to 1 increases the power rating of the primary by a factor of two. The voltage obtained from an extended delta is reduced by 12 percent over a nontapped winding. This increases the power rating of the secondaries by 12 percent. The load also requires an increase in power rating of 5 percent for each of the secondaries and a 1 percent increase for the primaries. The transformer is required to deliver rated power with input voltages from 2200 Vac to 2400 Vac. This increases the power rating of both the primary and the secondaries by 9 percent. The total equivalent power rating of the transformer is 3.9 MVA. This is a very favorable rating for this application, considering that constant output power is delivered over a voltage range of 4 to 1. Of this, a 2 to 1 voltage range is obtained from the switching of the converter connections.

Another feature of the transformer is the use of secondary shields to distribute impulse voltages generated by the operation of a crowbar. The crowbar shorts the dc output during load arcs. The shields are an alternative method to that of space-winding the top layer of each secondary coil.

III. Converter

The transformer generates two sets of six-phase outputs. Each six-phase output connects to two series full-wave bridge rectifiers to form a 12-pulse converter. The two 12-pulse converters are connected either in series or in parallel on the dc side. This provides a 2 to 1 range of output voltages. One range is from 31 kV to 62 kV, the other is 62 kV to 125 kV. Full utilization of the voltage and current rating of the rectifiers is made in this configuration because the parallel-to-series switching is made at the output of the converter. Performing the switching at the output of the rectifiers has the added advantage of not requiring an interphase balancing transformer. The three-phase transformer provides the necessary inductance to balance the currents between the two converters when operating in parallel.

The conversion of ac to dc generates harmonics both on the dc side of the converter and on the ac lines. For a perfect system, only characteristic harmonics are generated. These are of order np on the dc side and $np\pm1$ on the ac side, where n is the harmonic number and p is the converter pulse number. The assumption of a perfect system is never valid with real equipment. If a perfect system is represented by the positive sequence of electrical components, then imperfections can be represented by the negative sequence. Some imperfections are generated in the ac source and others are generated in the transformer. The generator also contains a negative sequence component.

The transformer requires windings with a turn ratio of $\sqrt{3}$. Since $\sqrt{3}$ is an irrational number, it can only be approximated by a fraction. This generates an asymmetry in the output voltage. The resulting negative phase sequence generates uncharacteristic harmonics. Another source of uncharacteristic harmonics is unequal inductances in each phase, but this is not a problem in this equipment due to the symmetry of the transformer coils.

The testing for dc harmonics was made with a voltage divider and a waveform analyzer. The transformer rectifier operated into a resistive load with no filter. The data compares the old unit at DSS-13 with the new unit. The old unit consisted of a delta primary and a tapped wye secondary with rectifiers connected for six-pulse operation.

The advantage of 12-pulse over six-pulse converters is a reduction by 12 dB in the principal component of the dc harmonic. The lowest frequency component for a six-pulse converter is $6f$, while for a 12-pulse it is $12f$, where f is the line frequency. For the old unit, the $6f$ component measured −21.3 dB referenced to the dc output voltage. For the new unit, the $12f$ component measured −35.8 dB. The theoretical value is −36 dB.

The advantages of a 12-pulse converter quite often are not realized due to uncharacteristic harmonics. Because the lowest

frequency components are the most difficult to filter, it is the value of these that must be reduced. The value of harmonics below the 12th are comparable for both units, except of course the sixth harmonic, which becomes an uncharacteristic harmonic for the 12-pulse converter. A value of –46.7 dB was measured for this harmonic in the new unit. This represents a reduction by a factor of 19 over the old unit.

The use of converters with increased pulse numbers is advantageous only if the uncharacteristic harmonics are kept low. The reduction obtained by the use of extended delta windings is significant and proves the advantages of tightly controlling the symmetry of the transformer coils. Both design and manufacturing are needed to achieve these results.

IV. Shielding

The stray capacitances were measured on the old transformer rectifier assembly at DSS-13. A measured value of 3.3 *nf* was obtained between the secondaries of the transformer and the tank. The measurement was repeated on the new unit and a value of 4.4 *nf* was obtained. The increased size of the new unit accounts for the larger value.

An electrostatic shield was placed inside the tank that encloses both the transformer and the rectifiers. This shield was then brought out to a separate terminal that will be connected to the return side of the load. The purpose is to prevent displacement currents from being conducted in the load. The shields in the new unit decreased the stray capacitance to the tank by 77 percent. (The actual value measured is 1.0 *nf*, compared to the unshielded unit of 4.4 *nf*.) This improvement is not as good as desired. The stray capacitances should be less than 100 *pf* if the ground currents from this source are going to be reduced to a value comparable to the body current of the newer klystrons; this requires an improvement in shielding of 97.7 percent from a unit without shielding. Although this level of improvement was not achieved, the 77 percent improvement represents an important step in decreasing and controlling ground currents.

The changes in tank current under operation are shown in Fig. 5(a) for the old unit and in Fig. 6(a) for the new unit. Note that the frequency is much higher for the new unit with no low-frequency components. Tests so far indicate no false triggering of the crowbar, although it is too early to conclude that the problem has been solved. Certainly, a lower value of ground current is desirable, but the design of a transformer would be made difficult if additional shielding were required. The use of box shields around the secondaries, although theoretically possible, would increase the size and weight of the transformer and consequently the cost. Such shielding interferes with the cooling of the coils, and also increases the margins, which in turn increases the size of the coils and the amount of iron for the core.

Measurement of ground currents at the generator was made in the ground return. The results are shown in Fig. 5(b) for the old unit and in Fig. 6(b) for the new unit. The transformer rectifier is a balanced three-phase load without a neutral connection. No zero sequence component is possible except as a result of capacitances between the transformer windings and the tank. Although an increase in current has been measured, this current should not affect the operation of the crowbar. No interference will be experienced as long as these currents do not pass in the load circuit.

V. Power Capability

The transformer rectifier is rated to deliver 2.25 MW to its load. Using this as the basis, a per-unit circuit of the 400-Hz supply is shown in Fig. 7. The transformer consists of four tap primaries connected in delta. The secondaries consist of four extended deltas. A total of 12 coils are mounted on the three legs of the core. Each converter is rated for one-quarter of the load, namely 562,500 watts. The cable between the generator and the transformer rectifier unit is estimated to have a 6 percent reactance. The generator is rated for 1.3 MVA into a 0.9 power factor load, and has a 1.0 per-unit reactance. The calculations assumed a second generator identical to the existing one now installed at the site. (This would provide a capacity of 2.6 MVA.) The procurement of a second generator with identical characteristics may be a problem because General Electric, the original manufacturer, has indicated that they will not manufacture another unit.

The converter power factor is 0.955 at the secondary of the transformer. The combining of converters improves the power factor on the line side of the transformer to 0.989. This was taken into account in calculating the per-unit parameters. The values of power factor and load vary with tap position. These values are summarized in Figs. 8 and 9.

A simulated load test was performed at the manufacturer's plant. The output of the rectifiers was short-circuited and the applied voltage was raised until rated load current was measured at the output. The test was performed on the worst tap for heating of the transformer winding. This type of test has a number of shortcomings. Among these are the disregard of core losses, winding resistance change due to frequency (the test was performed at 60 Hz), reverse-leakage current losses in the rectifiers, and rectifier switching losses. Even so, the test does account for the major losses in the unit. The input was measured as 25 kW.

For the first seven hours, the water coolant flow was set to zero. The temperature rose at a constant rate of 3 °C per hour with no sign of stabilization. The water coolant was turned on and the temperature stabilized at 24 °C above air-ambient and 11 °C above the water-inlet temperature. The amount of heat carried by the water was 14 kW; the remaining 11 kW was transferred through the tank walls to the air. The unit is rated to operate at 35 °C above air-ambient and 27 °C above water-inlet temperature. If it is assumed that the heat-transfer coefficient is constant over the temperature range of interest, then the unit is capable of dissipating 50 kW of internal heat. Since the worst-case calculated heat is 40 kW and the thermal time constant for this unit is much longer than the maximum temperature is ever expected to last in any one day, the transformer rectifier appears to be conservatively rated to handle 2.25 MW.

A load test was also performed at DSS-13. This test was at the 1-MW level because a higher power load was not available. The results are consistent with the short-circuit load test previously made at the vendor's plant.

The losses are summarized in Table 3. The copper losses are in close agreement with calculations. The core losses are much lower than calculated, and the measurement is suspect. The rectifier losses were not measured and the data is based on calculations.

VI. Impedance Test

From the data, the resistances were calculated so that comparisons could be made between the ac and dc values (see Table 4). The values are for all primaries connected in parallel and for one extended delta secondary short circuited. The values are referred to the primary. Table 4 lists only the values of one of the secondaries; the data for the other secondaries were equal to those listed within the accuracy of the measurements. Note some interesting results. The ac resistance is greater than the dc resistance, which is expected, but the ac resistance increased more rapidly than the dc resistance on the taps that included copper foil in the primary. (The primary winding consists of wire for the first 30 turns and foil for the remainder; the foil has higher ac resistance due to current concentration at the edges.) Note also that the leakage inductance decreases at the higher output voltages.

VII. Insulation

Testing of the winding layer insulation consisted of an induced voltage of 1.5 times the operating voltage for a duration of one minute. This was done with the rectifiers disconnected. A dielectric potential test of 150 kV rms was also applied to the rectifiers for a duration of one minute. Shields and the primary windings to ground were tested at 10 kV rms. These tests were performed to verify the integrity of the insulation. No arcing of the transformer rectifier unit was observed in any of the tests. (During the 150-kV test of the rectifiers, arcing was experienced with the cable connecting the test equipment to the unit.)

VIII. Output Voltages

The output voltage at light loads (E_{do}) is the basis for most calculations of converter performance. The values of E_{do} were calculated based on the turn ratio of the transformer. Measurements were made to check the validity of the calculated values; these are given in Table 5 in the "Data, kV" column.

The open-circuit output voltages were measured for the series connection only and are listed in the "No Load, kV" column in Table 5. The values for the series connection indicate an average of 15.5 percent over voltage above E_{do}, which is also the theoretical value of open circuit over voltage.

IX. Conclusion

The new transformer rectifier uses a number of techniques that provide advantages over previous designs. The use of 12-pulse converters generated from extended deltas has reduced the values of dc harmonic ripple. The use of series/parallel switching doubles the range of voltage output without any increase in the rating of the transformer or the rectifiers. The use of shielding has decreased ground currents, but further improvements in this area are still desired. Further design refinements are possible by extending these techniques.

Reference

[1] J. Arrillaga, D. Bradley, and P. Bodger, *Power System Harmonics*, New York: John Wiley & Sons, 1985.

Table 1. High-power transmitter output tubes

Klystron model no.	Power, kW	Beam V, kV	Beam I, A	Body I, mA	Band
X-3060	100.0	36.0	7.7	540	S-Band
VKS-8274	125.0	36.0	7	12	S-Band
X-3070	450.0	63.0	16.0	1200	S-Band
X-3075A	500.0	63.0	16.0	1200	S-Band
VKS-8276	500.0	60.0	17	15	S-Band
VA949	200.0	51.0	11	20	X-Band
VKX-7864	250.0	50.0	11	15	X-Band[a]
2 ea VKX-7864	500.0	50.0	22	30	X-Band[a]
4 ea VKX-7864	1000.0	50.0	44	60	X-Band[a]
Gyroklystron	400.0	100.0	10	25	Ka-Band[a]
Gyroklystron	1000.0	100.0	20	50	X-Band[a]

[a]Projected.

Table 2. Station transmitter supply capability

Station	Voltage, kV	Current, A max	Power output, MW	Generator rating, MVA
DSS-13	30–33 and 45–70	30.3	1	1.3
DSS-14	54–90	16.7	1	1.3[a]
DSS-43, DSS-63	42–76	21.7	1	1.3
New T/R	31–125	72.6	2.25	

[a]With capability of expansion to 2.6 with an additional generator.

Table 3. Losses

Tap number	Copper losses, W	Core losses[a], W	Diode loss, W
1	19100	1400	20440
2	16376	1800	18650
3	13660	2240	17150
4	12056	2640	15650
5	10372	3080	14400
6	8740	3840	13200
7	7080	4720	12070
8	5912	5880	11000

[a]These are very low values; the measurement may have been in error.

Table 4. Winding resistance and leakage inductance per section

Tap number	dc resistance, mohm	ac resistance, mohm	Inductance, μhenry
1	92.68	194.6	397.1
2	81.74	168.5	343.8
3	72.62	139.3	293.3
4	65.28	123.9	256.8
5	58.89	106.0	223.1
6	52.99	89.45	191.3
7	47.44	72.33	162.6
8	40.90	61.16	133.2

Table 5. Output dc voltages

	Series connection			Parallel connection	
Tap number	No load, kV	E_{do}, kV	Data, kV	E_{do}, kV	Data, kV
1	88.3	74.7	73.7	35.8	36.8
2	91.5	80	79.7	38.6	39.8
3	99.5	88.4	86.8	42	43.4
4	106	96	93	45.3	46.5
5	113	104	100	48.8	50.1
6	124	111	108.5	52.8	54.2
7	135	120	118	58	59.2
8	151	134	130	63.3	65.1

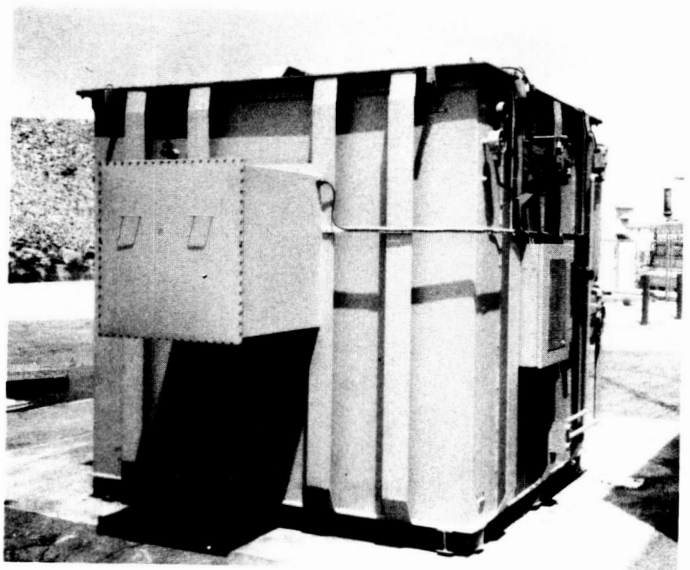
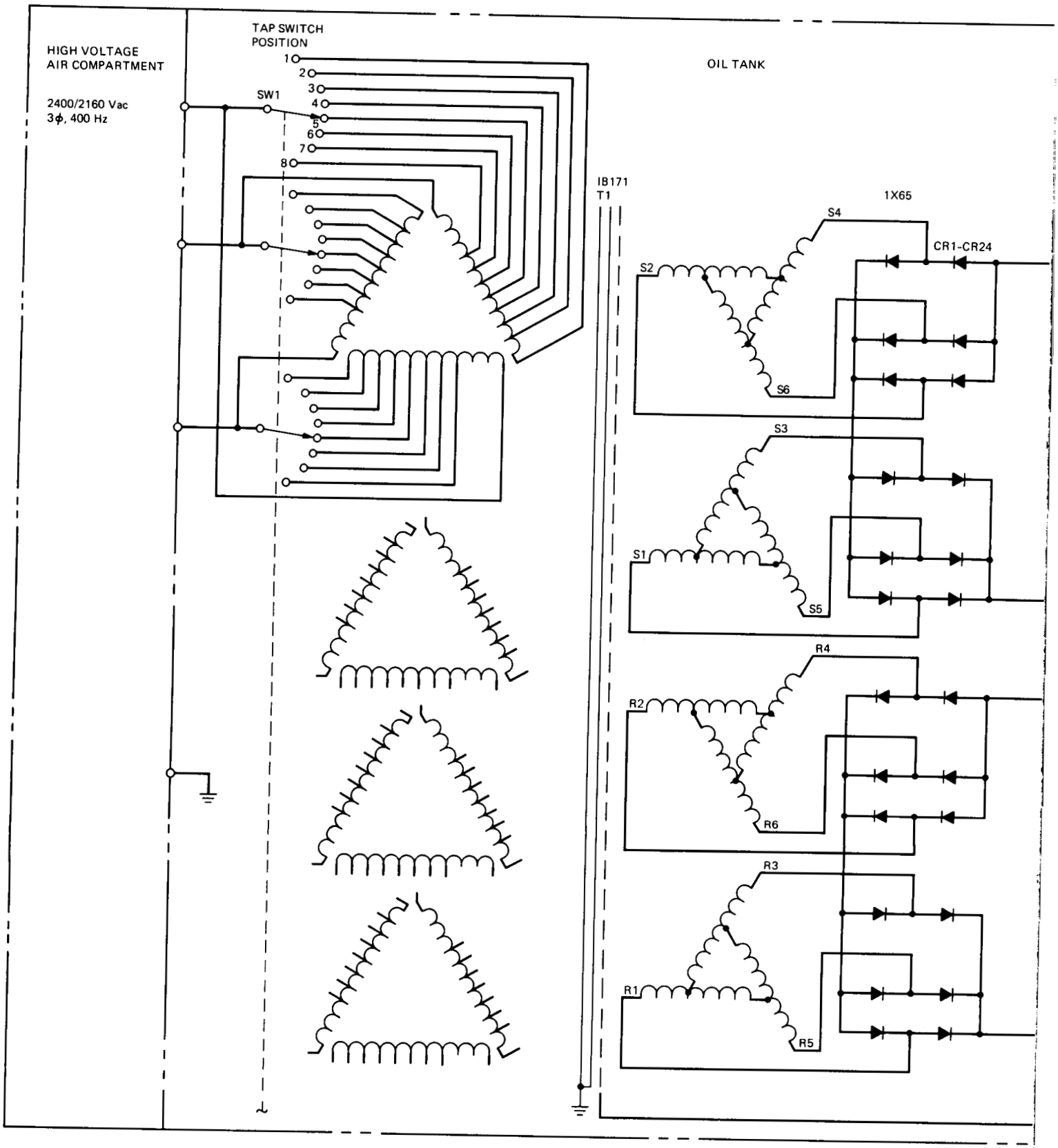
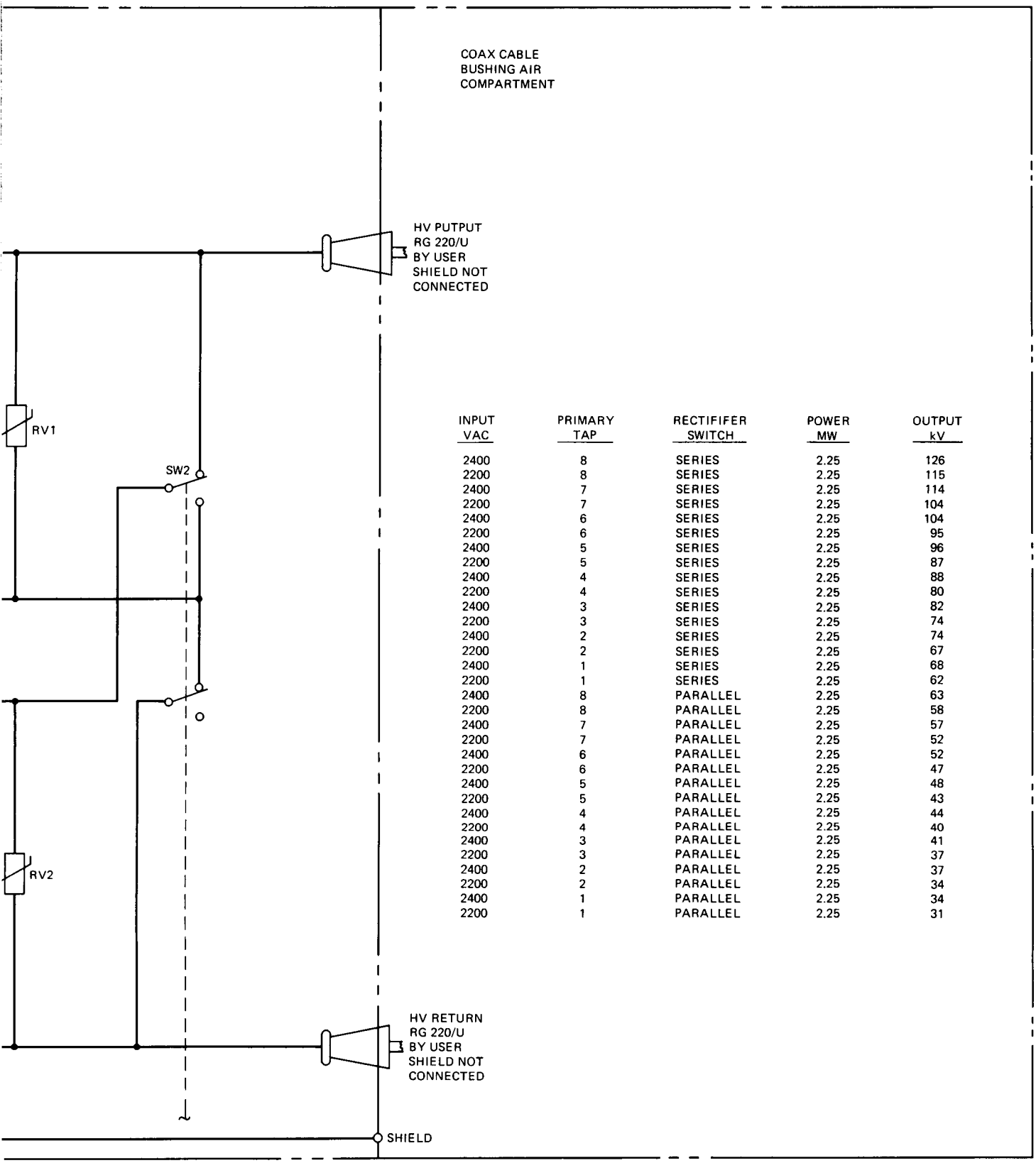


Fig. 1. Transformer rectifier assembly.

FOLDOUT FRAME



FOLDOUT FRAME



INPUT VAC	PRIMARY TAP	RECTIFIFER SWITCH	POWER MW	OUTPUT kV
2400	8	SERIES	2.25	126
2200	8	SERIES	2.25	115
2400	7	SERIES	2.25	114
2200	7	SERIES	2.25	104
2400	6	SERIES	2.25	104
2200	6	SERIES	2.25	95
2400	5	SERIES	2.25	96
2200	5	SERIES	2.25	87
2400	4	SERIES	2.25	88
2200	4	SERIES	2.25	80
2400	3	SERIES	2.25	82
2200	3	SERIES	2.25	74
2400	2	SERIES	2.25	74
2200	2	SERIES	2.25	67
2400	1	SERIES	2.25	68
2200	1	SERIES	2.25	62
2400	8	PARALLEL	2.25	63
2200	8	PARALLEL	2.25	58
2400	7	PARALLEL	2.25	57
2200	7	PARALLEL	2.25	52
2400	6	PARALLEL	2.25	52
2200	6	PARALLEL	2.25	47
2400	5	PARALLEL	2.25	48
2200	5	PARALLEL	2.25	43
2400	4	PARALLEL	2.25	44
2200	4	PARALLEL	2.25	40
2400	3	PARALLEL	2.25	41
2200	3	PARALLEL	2.25	37
2400	2	PARALLEL	2.25	37
2200	2	PARALLEL	2.25	34
2400	1	PARALLEL	2.25	34
2200	1	PARALLEL	2.25	31

Fig. 2. Transformer rectifier assembly detailed schematic.

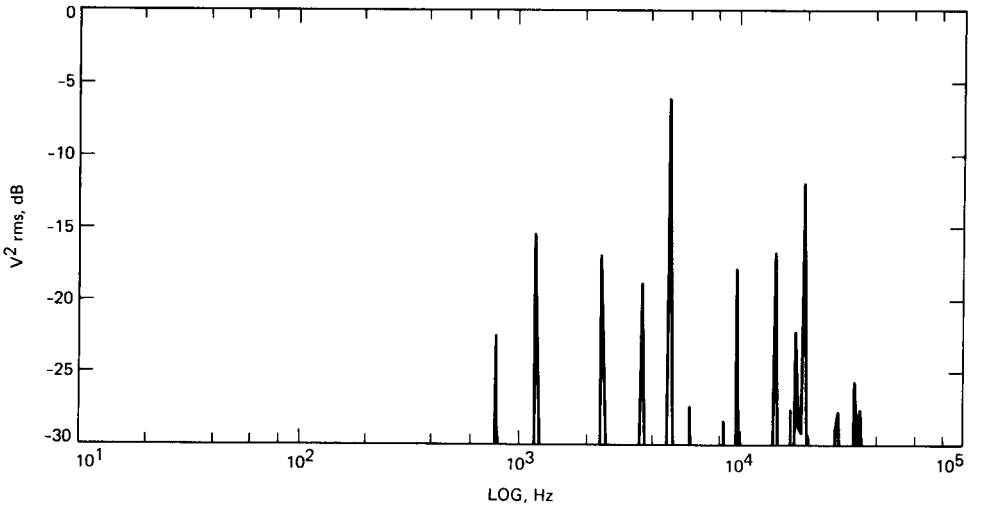


Fig. 3. New harmonic rectifier assembly dc harmonics.

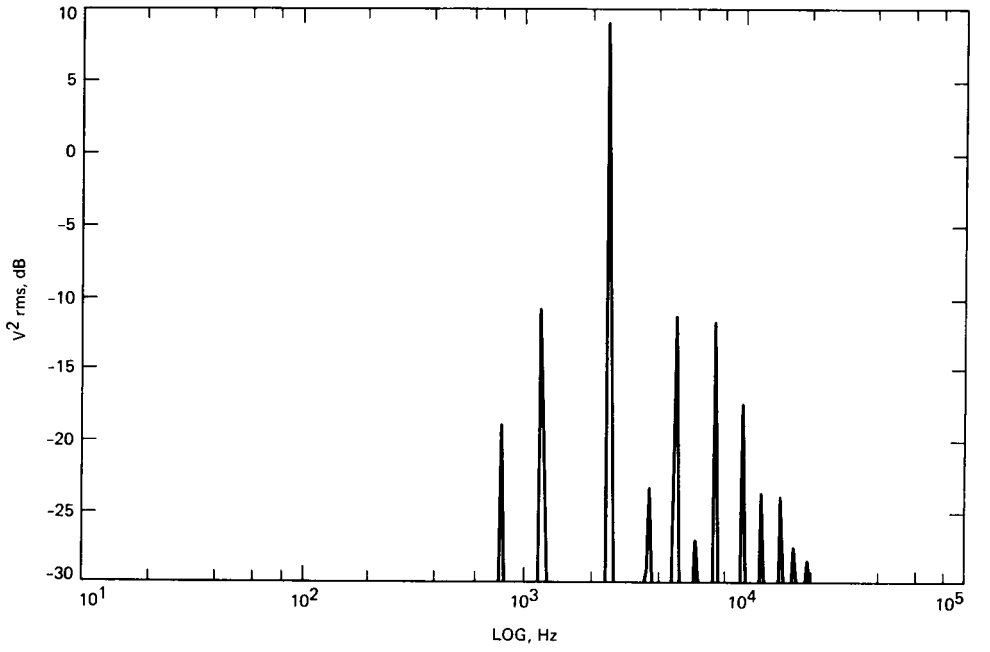


Fig. 4. Old harmonic rectifier assembly dc harmonics.

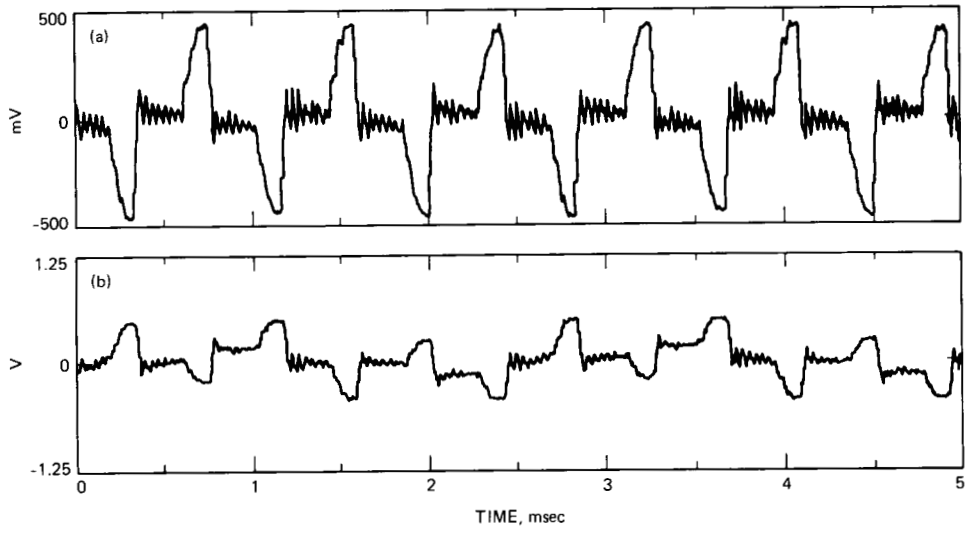


Fig. 5. Old harmonic rectifier assembly harmonics, (a) body, (b) generator.

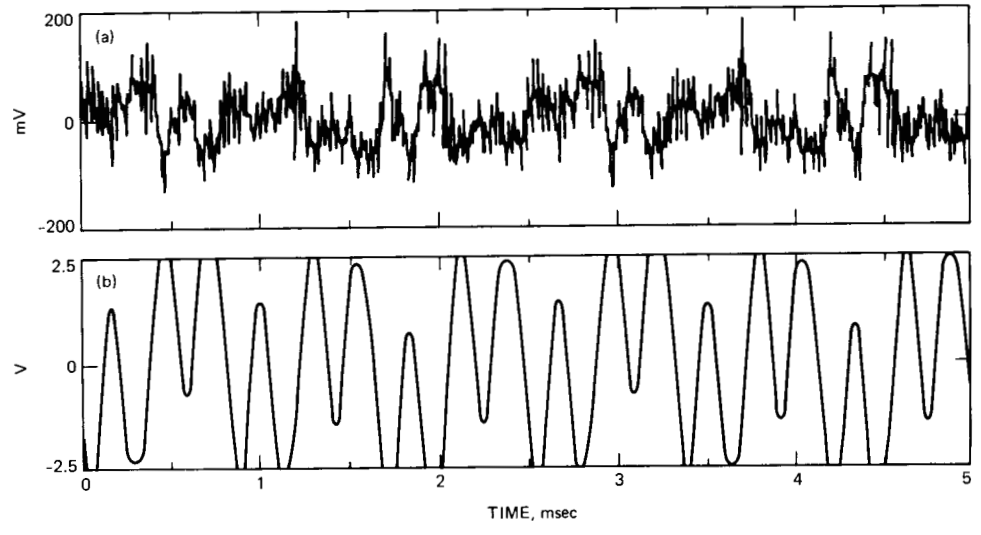


Fig. 6. New harmonic rectifier assembly harmonics, (a) body, (b) generator.

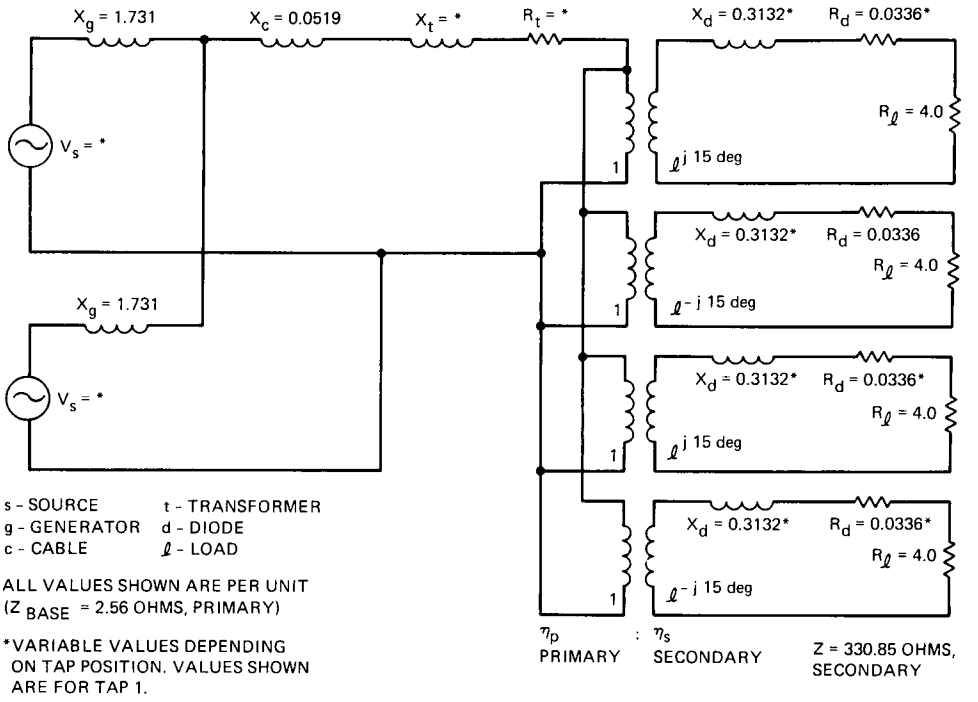


Fig. 7. 400-Hz power distribution per unit circuit.

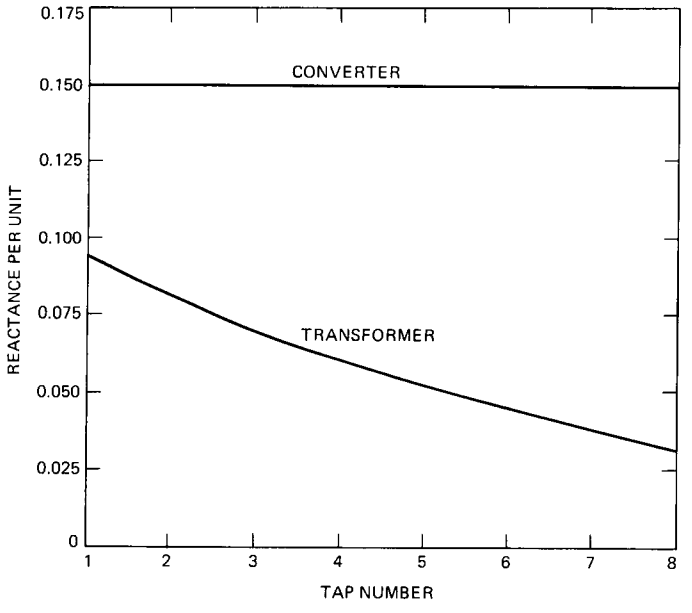


Fig. 8. Load reactance.

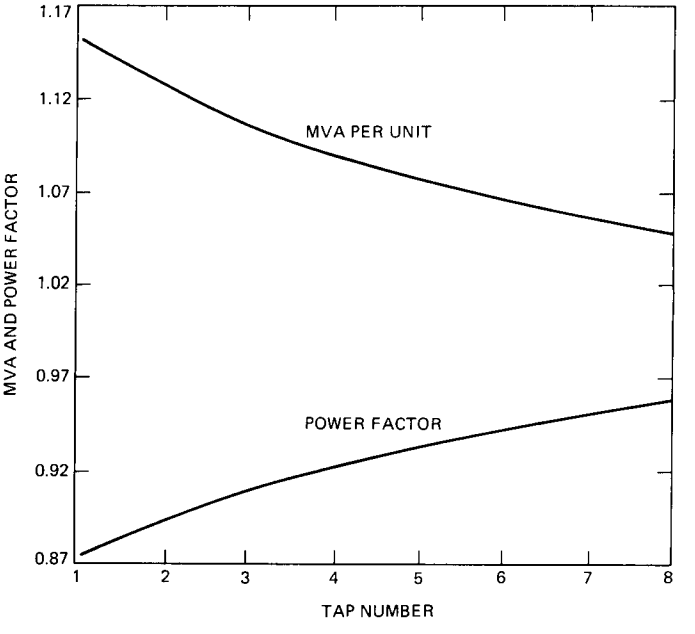


Fig. 9. Generator load.

TDA Progress Report 42-96

October – December 1988

On Sampling Band-Pass Signals

R. Sadr and M. Shahshahani
Communications Systems Research Section

~~In this article~~ four techniques for uniform sampling of band-pass signals are examined. The in-phase and quadrature components of the band-pass signal are computed in terms of the samples of the original band-pass signal. The relative implementation merits of these techniques are discussed with reference to the ~~DSN~~ Advanced Receiver.
Deep Space Network (DSN)

I. Introduction

In digital signal processing the input signal is reconstructed by first sampling it at a rate determined by the bandwidth of the signal and then using an interpolation formula. It is well known that for low-pass signals (i.e., supported in the frequency domain in the interval $[-W,W]$), the Nyquist sampling rate is sufficient for the reconstruction of the signal. In typical deep-space applications, one often encounters band-pass signals, i.e., signals whose support in the frequency domain lies in $I = I_1 \cup I_2$ where $I_1 = [f_c - W, f_c + W]$, $I_2 = -I_1$ (i.e., the signal vanishes outside the interval I), and f_c is the carrier frequency of the band-pass process. Such signals may be treated as low-pass and sampled at the Nyquist rate, however, this method is inefficient since f_c may be large compared to W. In this article four methods for more efficient sampling of band-pass signals are surveyed and their relative implementation merits are assessed.

II. Sampling Techniques

In the following it is assumed that the input signal is a real band-pass process centered at an intermediate frequency (IF), and it is desired to recover its in-phase and quadrature components.

Four sampling techniques are considered, namely:

(1) *I and Q baseband sampling with analog quadrature mixers (Fig. 1).* The input signal is mixed with the reference in-phase and quadrature component and low-pass filtered to reject the double frequency images produced by the mixing operation. Each channel (in-phase and quadrature) is independently sampled at the rate of $2W$ samples/sec. Note that the effective sampling rate is $4W$ samples/sec.

(2) *I and Q sampling with analog Hilbert transform (Fig. 2).* The input signal is Hilbert transformed, and both the input and its Hilbert transform are then sampled at the rate of $2W$ samples/sec. Here the effective sampling rate is also $4W$ samples/sec.

(3) *Band-pass sampling with digital quadrature mixers (Fig. 3).* The input signal is sampled at the rate of $4W$ samples/sec, and the input samples are then mixed with the samples of reference in-phase and quadrature components and then low-pass filtered to eliminate the double frequency images resulting from the mixing operation. This is performed by using a finite impulse response (FIR) low-pass filter. Since the output of the low-pass filter is bandlimited to $2W$, the output is deci-

mated (undersampled) by a factor of 2, thereby reducing the subsequent processing rate by 1/2. For band-pass sampling of the input signal it is assumed that the input signal is centered at an odd multiple of the bandwidth frequency. In practice, this is not a restrictive assumption since the IF frequency is normally chosen by the hardware design engineer.

(4) *Band-pass sampling with digital Hilbert transform (Fig. 4).* The input signal is sampled at the rate of $4W$ samples/sec, the input samples are then Hilbert transformed using a digital Hilbert transformer. The Hilbert transformed sequence and the input sequence are then mixed with the reference in-phase and quadrature components. For band-pass sampling of the input signal it is assumed that the input signal is centered at an odd multiple of the bandwidth frequency.

Note that cases (1) and (2) are applications of the Shannon-Whittaker theorem, while cases (3) and (4) are obtained from the band-pass sampling theorems discussed below.

III. Comparison of Sampling Methods

In this section the advantages and disadvantages of each of the sampling techniques described in the previous section are considered.

(1) *I and Q baseband sampling with analog quadrature mixers.*

Advantages:

(a) Since the sampling rate of each channel is $2W$ samples/sec, this technique requires the slowest possible A/D convertor and processing rate for the recovery of I and Q samples.

(b) The analog anti-aliasing filter design for this sampling technique is an ideal low-pass filter with a two-sided bandwidth of $2W$. Generally, low-pass analog filters are easier to build than their analog band-pass counterparts.

(c) Due to cost considerations, in some applications it is desirable to demodulate the signal directly from RF frequency to baseband with no intermediate stages. In such cases, this sampling method is the only known technique for recovering the in-phase and quadrature components.

Disadvantages:

(a) It is very difficult to achieve phase and amplitude balance in both in-phase and quadrature reference signals with analog quadrature mixers. Sinsky and Wang [1] have studied this effect when the input signal is simply a sinusoid at frequency f_0, and they show that the effect of unmatched phase or gain is to create an image at $-f_0$, where the power of this image is $A^2/4$ for amplitude mismatch, and $\phi^2/4$ for the phase mismatch. Here A and ϕ denote the fraction of amplitude imbalance and the phase difference in radians between the two channels, respectively. For example, to provide an image rejection ratio (IRR) of −50 dB due to the phase imbalance, the phase imbalance must be kept under 0.36 deg. In [2] a method is proposed for compensating for these imbalances. In applications where the signal-to-noise ratio is high, the consideration of IRR is not significant since the image power (at $-f_0$) is dominated by the channel noise.

(b) The appearance of spurious signals is another problem with analog implementation of quadrature mixers. Normally, high-speed analog mixers are high-speed choppers and produce odd and even harmonics of the carrier frequency. If these harmonics are not properly filtered, they could fold back into the baseband, and severely degrade the performance of the receiver.

(c) This technique requires two A/D convertors.

(2) *I and Q sampling with analog Hilbert transform.* Sometimes referred to as hybrids or 90-deg phase shifters, analog Hilbert transformers are hardly used in practice because of the difficulties inherent in their fabrication. The relative merits and disadvantages of this technique are similar to those of the previous case, except that here additional phase and amplitude imbalance is introduced by the analog Hilbert transformer if it exhibits non-ideal characteristics.

(3) *Band-pass sampling with digital quadrature mixers.*

Advantages:

(a) Since quadrature mixing is done in the digital domain, the phase or amplitude imbalance problems discussed earlier for the baseband sampling with analog quadrature mixers do not appear here.

(b) Low-pass filtering operation is done in the digital domain using FIR filters. These filters are linear phase filters, i.e., they introduce a constant group delay in the output I and Q samples. This is particularly important in applications where ranging or Doppler information must be extracted from the received signal. Digital filters are inherently more robust and flexible than their analog counterparts. The bandwidth of the filter can be easily modified by changing the coefficients of the discrete filter. Furthermore, a special class of filters [3]

called half-band filters (HBF) reduces the computational complexity and the processing rate of this sampling technique by a factor of two.

(c) Only one A/D convertor is required.

(d) If the sampling period is exactly $1/(4f_c)$, then the reference in-phase and quadrature components reduce to an alternating sequence.

Disadvantages:

(a) Faster A/D conversion (e.g., aperture conversion time) is required since the sampling rate is at least at $4W$, as opposed to $2W$ for the baseband sampling case. This translates into stricter design requirements for the A/D design parameters, such as the sample and hold, and aperture time.

(b) Requires a band-pass anti-aliasing filter prior to A/D conversion. As pointed out earlier, analog band-pass filters are more difficult to fabricate than their low-pass counterparts.

(4) *Band-pass sampling with digital Hilbert transform*. This technique is similar to the previous one with the additional disadvantage that the hardware realization of the ideal digital Hilbert transformer requires greater precision (more bits) than that of a digital low-pass filter. The implementation of an ideal digital Hilbert transform is discussed in [4].

IV. Technical Background

A. Analog Signals

Let $O(f_c,W)$ denote the space of all square-integrable complex-valued functions supported in $I = I_1 \cup I_2$, and let $\Omega(f_c,W)$ denote its Fourier transform, i.e., all functions representable in the form

$$x(t) = \int X(\lambda) \exp(2\pi j \lambda t)\, d\lambda \qquad (1)$$

where $X \in O(f_c,W)$. Here f_c represents the carrier frequency. In [5] and [6] the following theorem is proved, which can serve as the basis for the reconstruction of the signal from its samples:

Theorem 1. Let

$$\phi(t) = \int_I \exp(2\pi j \lambda t)\, d\lambda$$

(a) If $T = 1/4W$ and $f_c = (2k + 1)W$ for some positive integer k, then

$$\int \phi(t - nT)\, \phi(t - mT)\, dt = c\, \delta_{mn}$$

for some non-zero constant c, and the sequence $\{\phi(t - nT), n \in \mathbf{Z}(=\text{integers})\}$ is complete in $\Omega(f_c,W)$. The condition $f_c = (2k + 1)W$ is also necessary for orthogonality and completeness of the sequence $\{f(t - nT), n \in \mathbf{Z}\}$.

(b) If $T_1 = (1/2)W$, $f_c = kW$, $\alpha = (1/(4f_c))(2I + 1)$, ($I$ integer), then $\{\phi(t - nT_1), n \in \mathbf{Z}\} \cup \{\phi(t - nT_1 - \alpha), n \in \mathbf{Z}\}$ is complete and orthogonal in $\Omega(f_c,W)$.

Theorem 1 provides two methods for sampling. Part (a) gives the expansion

$$x(t) = \left(\frac{1}{c}\right) \sum x(nT)\, \phi(t - nT) \qquad (2)$$

and the $x(nT)$ terms are the sampled values. For obvious reasons this is called uniform sampling. Quadrature sampling is the technical term for expansion of $x(t)$ in terms of the sequence given in (b). Here one has

$$x(t) = \left(\frac{1}{4W}\right) \sum x(nT_1)\, \phi(t - nT_1) + \left(\frac{1}{4W}\right) \sum x(nT_1 + \alpha)\, \phi(t - nT_1 - \alpha) \qquad (3)$$

As noted earlier, if the RF signal is mixed down by an RF down convertor, then the IF frequency can be adjusted to satisfy the requirements $f_c = (2k + 1)W$ or $f_c = kW$ in Theorem 1. In general, one does not expect any relation between f_c and W, and Theorem 1 is not directly applicable. To remedy this situation, let

$$kW < f_c < (k + 1)W$$

Either k or $k + 1$ is even, say $k = 2I$. If I is odd, regard the band-pass signal $X(\lambda)$ as supported in $I' = I_1' \cup I_2'$ with $I_1' = [f_c' - 2W, f_c' + 2W]$ and $f_c' = kW$, $I_2' = -I_1'$. Then apply Theorem 1, sample at points $(1/(8W))$ and apply part (a) to reconstruct the function. If I is even, then use the same interval I', sample $x(t)$ at the points $n/4W$ and $\beta + (n/4W)$ where $\beta = (2m + 1)/4kW$, m is any fixed integer, and use the expansion of part (b).

It is sometimes convenient to express $x(t)$ in the form

$$x(t) = \alpha(t) \cos 2\pi f_c t - \beta(t) \sin 2\pi f_c t \qquad (4)$$

where α and β are Fourier transforms of band-limited functions. Here α and β are called the quadrature and in-phase components of the signal. To obtain the expansion of Eq. (4), first note that

$$\phi(t) = -\left(\frac{2}{\pi t}\right) \sin 2\pi W t \cos 2\pi f_c t$$

and substitute the expansion given in part (a) to obtain

$$\alpha(t) = \left(\frac{-1}{2\pi W}\right) \sum x(nT) \left(\frac{\sin 2\pi W(t-nT)}{(t-nT)}\right) \cos 2\pi f_c nT$$

$$\beta(t) = \left(\frac{-1}{2\pi W}\right) \sum x(nT) \left(\frac{\sin 2\pi W(t-nT)}{(t-nT)}\right) \sin 2\pi f_c nT$$

The fact that α and β are Fourier transforms of band-limited functions is a straightforward application of the Paley-Weiner theorem.

Since in practice one can only compute finitely many terms, the problem of rate of convergence of the interpolating series is a significant one. The following proposition and the remark following it provide the answer to this problem:

Proposition 1. If the function $X(\lambda)$ is twice continuously differentiable, then the series in Eqs. (2) and (3) converge absolutely and uniformly in t. Furthermore, in case (a)

$$\left| x(t) - \sum_N \right| < c' \frac{\|X''\|}{N}$$

where Σ_N denotes the sum from $-N$ to N in Eq. (1), c' is a constant depending only on W, and $\|X''\|$ is the L^2 norm of the second derivative of X. A similar estimate holds in case (b).

Proof. Integrating Eq. (1) by parts twice and using Cauchy-Schwartz one obtains, for some constant c'' depending only on W,

$$|x(t)| < \left(\frac{c''}{t^2}\right) \|X''\|$$

Substituting the above estimate for $t = nT$ in Eq. (2) and using the upper bound $(2/\pi)$ for ϕ, the desired results are obtained after some simple manipulations.

Remark. The proof of Proposition 1 also shows that the estimate above can be replaced by

$$\left| x(t) - \sum_N \right| < c' \frac{\|X^{(k+1)}\|}{N^k}$$

where $X^{(k+1)}$ denotes the $(k+1)$th derivative of X. Therefore, it may appear that the right-hand side can be made arbitrarily small by taking k to be sufficiently large. That this is not the case follows easily from the fact that $\|X^{(k+1)}\|$ has very rapid growth with k. More precisely, since x is analytic, for every M there is $\eta > 0$ such that

$$\left(\int^{-M} + \int_M\right) |x(t)|^2 \, dt > \eta \int |x(t)|^2 \, dt$$

Therefore

$$\|X^{(k)}\|^2 > \left(\int^{-M} + \int_M\right) |t|^{2k} |x(t)|^2 \, dt > \eta M^{2k} \|x\|^2$$

so that $\|X^{(k)}\|$ grows at least as fast as M^k. In the actual numerical calculation of the second derivative of X one may use the approximation

$$\frac{\left(X(\lambda + 2\delta) - 2X(\lambda + \delta) + X(\lambda)\right)}{\delta^2}$$

for $X''(\lambda)$ or approximately evaluate

$$\int |t|^4 |x(t)|^2 \, dt = \|X''\|^2$$

One may also use a combination of the Fourier and Hilbert transforms to reconstruct the signal in the time domain from its sampled values. Recall that the Hilbert transform of X is

$$\hat{x}(t) = \int \sin(\lambda) \exp(2\pi j \lambda t) X(\lambda) \, d\lambda$$

The following theorem describes how combination of the analog Fourier and Hilbert transforms can be used for the reconstruction from sampled values:

Theorem 2. Assume that the band-pass signal $x(t)$ and its transform $X(\lambda)$ are real. The signal can then be reconstructed from the sampled values $x(n/2W)$ and the Hilbert transform $\hat{x}(n/2W)$ by the formula

$$x(t) = \sum (-1)^n \left[\frac{\sin 2\pi W\left(t - \left(\frac{n}{2W}\right)\right)}{2\pi W\left(t - \left(\frac{n}{2W}\right)\right)}\right] A(n) \cos 2\pi f_c t$$

$$+ \sum (-1)^n \left[\frac{\sin 2\pi W\left(t - \left(\frac{n}{2W}\right)\right)}{2\pi W\left(t - \left(\frac{n}{2W}\right)\right)}\right] B(n) \sin 2\pi f_c t$$

where

$$A(n) = y_1\left(\frac{n}{2W}\right)\cos\left(\frac{2\pi f_c n}{2W}\right) + z_1\left(\frac{n}{2W}\right)\sin\left(\frac{2\pi f_c n}{2W}\right)$$

$$B(n) = y_1\left(\frac{n}{2W}\right)\sin\left(\frac{2\pi f_c n}{2W}\right) - z_1\left(\frac{n}{2W}\right)\cos\left(\frac{2\pi f_c n}{2W}\right)$$

$$y_1\left(\frac{n}{2W}\right) = \left(\frac{1}{2}\right)x\left(\frac{n}{2W}\right)$$

$$z_1\left(\frac{n}{2W}\right) = \left(\frac{1}{2j}\right)\hat{x}\left(\frac{n}{2W}\right)$$

(Notice that since $X(-\lambda) = X(\lambda)$ and X is real, $\hat{x}$ is purely imaginary and z_1 is real.)

Proof. Let χ_1 (resp. χ_2) denote the indicator function of the set I_1 (resp. I_2), and set $X_i(\lambda) = \chi_i(\lambda)X(\lambda)$. Let x_i denote the Fourier transform of X_i. Now $X_1(\lambda)$ admits of the Fourier series expansion

$$X_1(\lambda) = \sum a_n \exp\left(\frac{2\pi jn\lambda}{2W}\right) \tag{5}$$

The coefficient a_n is given by

$$a_n = \left(\frac{1}{2}W\right)\int X_1(\lambda)\exp\left(\frac{-2\pi jn\lambda}{2W}\right)d\lambda$$

i.e.,

$$a_n = \left(\frac{1}{2}W\right)x_1\left(\frac{n}{2W}\right)$$

Substituting Eq. (5) into Eq. (1) and assuming change of order of summation and integration is permissible, one obtains after a simple calculation

$$x_1(t) = \sum x_1\left(\frac{n}{2W}\right)K_1(n,t)$$

where

$$K_1(n,t) = \frac{\exp\left(2\pi ja\left(t - \frac{n}{2W}\right)\right)\sin 2\pi W\left(t - \frac{n}{2W}\right)}{2\pi W\left(t - \frac{n}{2W}\right)}$$

One then decomposes $x_i = y_i + jz_i$ into its real and imaginary parts. Since $x(t)$ is real, x_2 is the complex conjugate of x_1. Substituting in $x = x_1 + x_2$, the desired expansion is obtained.

B. Digital Signals

The reconstruction formulae for the digital case are similar to those for the analog signal. To see this recall that by reconstruction in the digital domain we mean an interpolation formula for $x(t)$ in terms of the sampled values $x(n/2W)$ and the discrete Hilbert transform (DHT) of $x(n/2W)$. By DHT we mean

$$\tilde{x}(t) = \left(\frac{1}{2}\pi j\right)\int \operatorname{sign}(\omega)\,\xi(\omega)\exp(2\pi j\omega t)\,d\omega$$

where $\xi(\omega)$ is the discrete Fourier transform of $x(n/2W)$. Since

$$X(\lambda) = \left(\frac{1}{2}W\right)\sum x\left(\frac{n}{2W}\right)\exp\left(\frac{2\pi j\lambda}{2W}\right)$$

$X(\lambda)$ is given as the discrete Fourier transform of $x(n/2W)$, and hence the interpolation formula for the Hilbert transform is implementable in the digital domain.

C. Non-Deterministic Signals

The above considerations are also applicable to the case where the signal is not deterministic. To be more precise, replace $x(t)$ by a possibly complex-valued stationary process $x(t,\omega)$, or simply $x(t)$, where ω lies in some probability space Ω. We assume that $E\{x(t)\} = 0$ for all t, and the autocorrelation function

$$R(s,t) = R(s-t) = E\{x(t)x(s)^*\}$$

is the Fourier transform of a band-limited function $s(\lambda)$ supported in the interval $[-W,W]$. We want to reconstruct the process, at least for almost all ω. This is possible because the sample paths of such processes are, with probability 1, Fourier transform functions supported in $[-W,W]$ and therefore entire functions. This is the content of a theorem of Belyaev which can be stated as follows [7].

Theorem 3. If R is an entire function of exponential type with the exponent not exceeding W, then with probability 1 all sample paths of the process $x(t)$ are entire functions of exponential type with the exponent not exceeding W.

Therefore, for such a process for almost all ω, $x(t) = x(t,\omega)$ can be extended to the complex plane as a function of t and is in fact the inverse Fourier transform of a band-limited distribution. If it is furthermore assumed that R is the inverse Fourier transform of a continuous function supported in $[-W,W]$, then with probability 1, $x(t)$ is the inverse Fourier transform of a continuous function supported in $[-W,W]$. This implies that the sampling theorem for signals supported in

$[-W,W]$ is applicable to the sample paths of the noise process and for almost all ω, $x(t) = x(t,\omega)$ can be reconstructed from its sampled values at intervals of length $(1/(2W))$ by the same formulae as in the deterministic case.

V. Conclusion

It has been found that band-pass sampling using digital quadrature mixers is the most robust technique for Deep Space Network (DSN) applications. In deep space applications the signal-to-noise ratio (SNR) is extremely low, e.g., the Advanced Receiver performance threshold is at 0 dB with a carrier-to-noise power of -75 dB with a 15 MHz bandwidth. In DSN applications it is necessary to detect telemetry symbols and track signal phase very accurately for ranging and Doppler measurement in order to determine the deep space probe's position and velocity. Thus, the receiving system cannot tolerate any significant loss due to filtering or phase distortion. Band-pass sampling with digital quadrature mixers can meet these requirements since it does not suffer from the phase and amplitude imbalance which is inherent in I and Q baseband sampling.

References

[1] A. I. Sinsky and P. C. P. Wang, "Error Analysis of a Quadrature Coherent Detection Processor," *IEEE Trans. Aerospace Electronic Systems*, vol. AES-10, pp. 880–883, November 1974.

[2] F. E. Churchill et al., "Correction of I and Q Errors in a Coherent Processor," *IEEE Trans. on Aerospace Electronic Systems*, vol. AES-17, no. 1, pp. 131–137, January 1981.

[3] R. Sadr and W. Hurd, "Digital Carrier Demodulation for the DSN Advanced Receiver," *TDA Progress Report 42-93*, vol. January–March, Jet Propulsion Laboratory, Pasadena, California, pp. 45–63, May 15, 1988.

[4] A. V. Oppenheim and R. W. Shafer, Digital Signal Processing, New Jersey: Prentice Hall, 1975.

[5] J. L. Brown, Jr., "On Quadrature Sampling of Bandpass Signals," *IEEE Trans. Aerospace Electronic Systems*, vol. AES-15, no. 3, pp. 366–370, May 1979.

[6] J. L. Brown, Jr., "First-Order Sampling of Bandpass Signals–A New Approach," *IEEE Trans. Information Theory*, vol. IT-26, no. 5, pp. 613–615, September 1980.

[7] Y. K. Belyayev, "Analytic Random Processes," *Theory of Probability and Its Applications*, (English Edition), vol. 4, pp. 402–409, 1959.

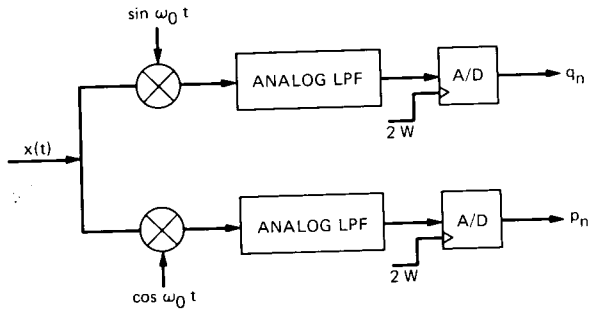


Fig. 1. I and Q baseband sampling with analog quadrature mixers.

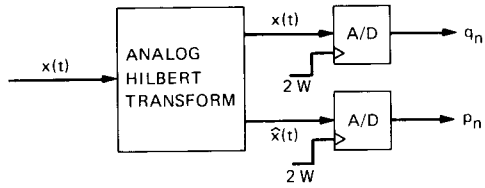


Fig. 2. I and Q baseband sampling with analog Hilbert transform.

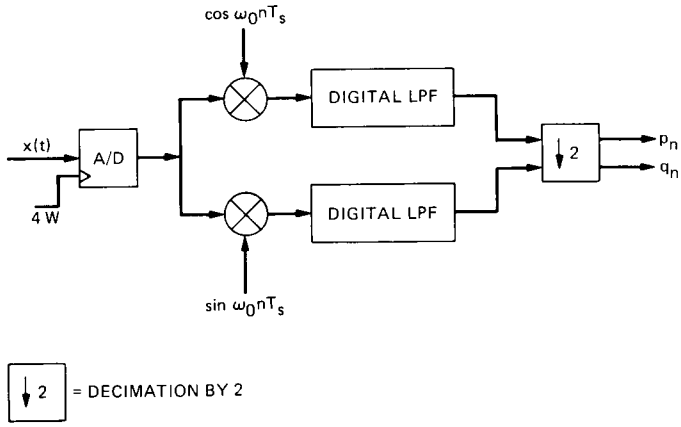


Fig. 3. Band-pass sampling with digital quadrature mixers.

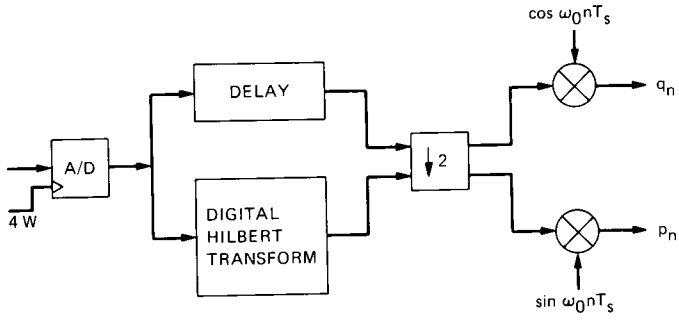


Fig. 4. Band-pass sampling with digital Hilbert transform.

The Use of Interleaving for Reducing Radio Loss in Convolutionally Coded Systems

D. Divsalar
Communications Systems Research Section

M. K. Simon
Telecommunications Systems Section

J. H. Yuen
Telecommunications Science and Engineering Division

~~In this article~~ the use of interleaving after convolutional coding and deinterleaving before Viterbi decoding is proposed. This effectively reduces radio loss at low-loop ~~SNRs~~ signal to noise ratios (SNRs) by several decibels and at high-loop SNRs by a few tenths of a decibel. Performance of the coded system can further be enhanced if the modulation index is optimized for this system. This will correspond to a reduction of bit SNR at a certain bit error rate for the overall system. The introduction of interleaving/deinterleaving into communication systems designed for future deep space missions does not substantially complicate their hardware design or increase their system cost.

I. Introduction

In analyzing the performance of coherent receivers of convolutionally encoded phase modulation, one often makes the simplifying assumption that the reference signal used for demodulation is perfectly phase synchronized to the transmitted signal, i.e., one assumes ideal coherent detection [1].

In a practical receiver, such as that used by NASA's Deep Space Network, the coherent demodulation reference is derived from a carrier synchronization subsystem, e.g., a type of phase-locked loop or Costas loop, resulting in a performance degradation due to the phase error between the received signal and the locally generated reference. Since this subsystem forms its demodulation reference from a noise-perturbed version of the transmitted signal, the phase error is a random process. The manner in which this process degrades the system error probability performance depends on the ratio of data rate to loop bandwidth, i.e., the rate of variation of the phase error over the data symbol interval [2, 3].

In this article, the above degradation in signal-to-noise ratio (SNR) performance (often referred to as *radio* or *noisy reference loss*) is discussed, and it is shown how it can be reduced by employing interleaving/deinterleaving. Specific closed form results are derived for both discrete and suppressed carrier systems and the differences between the two are discussed and numerically illustrated.

II. Upper Bound on the Average Bit Error Probability Performance

A. Perfect Carrier Phase Synchronization

For a convolutionally encoded binary phase-shift-keyed (BPSK) modulation transmitted over a perfectly phase-synchronized additive white Gaussian noise (AWGN) channel (Fig. 1), an upper bound on the average bit error probability is given as [1]

$$P_b \leqslant \sum_{\underline{x},\hat{\underline{x}} \in C} \sum a(\underline{x},\hat{\underline{x}})\, p(\underline{x})\, P(\underline{x} \to \hat{\underline{x}}) \tag{1}$$

where $a(\underline{x}, \hat{\underline{x}})$ is the number of bit errors that occurs when the sequence $\underline{x}$ is transmitted and the sequence $\hat{\underline{x}} \neq \underline{x}$ is chosen by the decoder,[1] $p(\underline{x})$ is the a *priori* probability of transmitting $\underline{x}$, and C is the set of all coded sequences. Also, in Eq. (1), $P(\underline{x} \to \hat{\underline{x}})$ represents the pairwise error probability, i.e., the probability that the decoder chooses $\hat{\underline{x}}$ when indeed $\underline{x}$ was transmitted. The upper bound of Eq. (1) is efficiently evaluated using the transfer function bound approach [1].

In general, evaluation of the pairwise error probability depends on the proposed decoding metric, the presence or absence of channel state information (CSI), and the type of detection used, i.e., coherent versus differentially coherent. For the case of interest here, namely, coherent detection with no CSI and a Gaussian metric (optimum for the AWGN channel), it is well known [1] that the pairwise error probability is given by

$$P(\underline{x} \to \hat{\underline{x}}) \leqslant \exp\left\{-\frac{E_s}{N_0}\, d_H(\underline{x},\hat{\underline{x}})\right\} \tag{2}$$

where

$$d_H(\underline{x},\hat{\underline{x}}) = \frac{1}{4}\sum_n \left|x_n - \hat{x}_n\right|^2 \tag{3}$$

represents the Hamming distance between $\underline{x}$ and $\hat{\underline{x}}$, i.e., the number of symbols in which the sequences $\underline{x}$ (the correct one) and $\hat{\underline{x}}$ (the incorrect one) differ. In Eq. (2), E_s is the energy-per-output coded symbol and N_0 is the single-sided noise spectral density.

B. Imperfect Carrier Phase Synchronization

1. Discrete Carrier (No Interleaving). When a carrier phase error $\phi(t)$ exists between the received signal and the locally generated demodulation reference, then the result in Eq. (2) is modified as follows.

Assuming the case in which the data symbol rate $1/T_s$ is high compared to the loop bandwidth B_L, then $\phi(t)$ can be assumed constant (independent of time) over a number of symbols on the order of $1/B_L T_s$. In this case, let $\phi(t) = \phi$. Since the decoder has no knowledge of ϕ, the decoding metric can make no use of this information and as such is *mismatched* to the channel. Under these conditions, it can be shown (see the Appendix) that using the maximum-likelihood metric for a perfectly phase-synchronized AWGN, one obtains

$$P(\underline{x} \to \hat{\underline{x}} \mid \phi; \lambda) \leqslant \begin{cases} \dfrac{1}{2}\exp\left\{-\dfrac{E_s}{N_0}\, 4\lambda(\cos\phi - \lambda)\, d_H(\underline{x},\hat{\underline{x}})\right\}; & 0 \leqslant |\phi| \leqslant \dfrac{\pi}{2} \\ 1; & \dfrac{\pi}{2} \leqslant |\phi| \leqslant \pi \end{cases} \tag{4}$$

where $\lambda \geqslant 0$ is a parameter to be optimized. Note that for $\phi = 0$, the expression $4\lambda(1 - \lambda)$ is maximized by the value $\lambda = 1/2$, which when substituted in Eq. (4) yields Eq. (2) as it should.

Letting $p(\phi)$ denote the probability density function (p.d.f.) of the phase error ϕ, the average bit error probability is upper bounded by[2]

$$P_b \leqslant \sum_{\underline{x},\hat{\underline{x}} \in C} \sum a(\underline{x},\hat{\underline{x}})\, p(\underline{x}) \min_{\lambda} E_\phi\left\{P(\underline{x} \to \hat{\underline{x}} \mid \phi; \lambda)\right\} \tag{5}$$

where $E_\phi\{\cdot\}$ denotes statistical averaging over the p.d.f. $p(\phi)$. Using Eq. (4), the statistical average required in Eq. (5) becomes

[1] For simplicity of notation, the sequences $\underline{x}$ and $\hat{\underline{x}}$ are assumed to be normalized such that their elements take on values ± 1.

[2] Later on a tighter bound for this case is presented by optimizing on λ prior to performing the expectation over ϕ.

$$E_\phi\{P(\underline{x}\to\hat{\underline{x}}\,|\,\phi;\lambda)\} =$$

$$\int_{-\pi/2}^{\pi/2}\frac{1}{2}\exp\left\{-\frac{E_s}{N_0}\,4\lambda(\cos\phi-\lambda)\,d_H(\underline{x},\hat{\underline{x}})\right\}p(\phi)\,d\phi$$

$$+2\int_{\pi/2}^{\pi}p(\phi)\,d\phi \tag{6}$$

2. Discrete Carrier (With Interleaving). Ordinarily, one thinks of using interleaving/deinterleaving to break up the effects of error bursts in coded communication systems. One can gain an intuitive notion of how it may be applied in systems with noisy carrier phase reference by considering the $\cos\phi$ degradation factor as an "amplitude fade" whose duration is on the order of $1/B_L T_s$ symbols. Thus, if we break up this "fade" by interleaving to a depth on the order of $1/B_L T_s$, then, after deinterleaving, the degradation due to $\cos\phi$ will be essentially *independent* from symbol to symbol. From a mathematical standpoint, this is equivalent to replacing Eq. (4) by[3]

$$P(\underline{x}\to\hat{\underline{x}}\,|\,\underline{\phi};\lambda)\leqslant$$

$$\begin{cases}\dfrac{1}{2}\exp\left\{-\dfrac{E_s}{N_0}\displaystyle\sum_{n=1}^{d_H}4\lambda(\cos\phi_n-\lambda)\right\}; & \displaystyle\sum_{n=1}^{d_H}\cos\phi_n>0\\[2ex] 1; & \displaystyle\sum_{n=1}^{d_H}\cos\phi_n\leqslant 0\end{cases} \tag{7}$$

where the ϕ_n variables are independent identically distributed (i.i.d.) random variables with p.d.f. $p(\phi)$, and $\underline{\phi}$ refers to the vector whose components are ϕ_ns. The derivation of Eq. (7) is given in the Appendix. The expectation required in Eq. (5) now involves computation of multidimensional integrals over regions of $\underline{\phi}$ corresponding to the inequalities in Eq. (7). In these regions, since the intervals of integration per dimension are *dependent* on one another, the expectation required in Eq. (5) is extremely difficult to compute.

Thus, instead we turn to a looser upper bound on conditional pairwise error probability, which has the advantage of not having to separate the multidimensional integration required in Eq. (5) into two disjoint regions. Indeed, it is straightforward to see that the right-hand side of Eq. (7) is upper bounded by the exponential in its first line (without the factor of 1/2) over the *entire* domain of $\underline{\phi}$, i.e., $\{\phi_n\in(-\pi,\pi);n\in\eta\}$. Hence,

$$P(\underline{x}\to\hat{\underline{x}}\,|\,\underline{\phi};\lambda)\leqslant\exp\left\{-\frac{E_s}{N_0}\sum_{n=1}^{d_H}4\lambda(\cos\phi_n-\lambda)\right\}$$

$$=\prod_{n=1}^{d_H}\exp\left\{-\frac{E_s}{N_0}\,4\lambda(\cos\phi_n-\lambda)\right\} \tag{8}$$

which is identically equal to the Chernoff bound. Now, substituting Eq. (8) into Eq. (5) gives the much simpler result

$$E_\phi\{P(\underline{x}\to\hat{\underline{x}}\,|\,\phi;\lambda)\} = \prod_{n=1}^{d_H}\int_{-\pi}^{\pi}\exp\left\{-\frac{E_s}{N_0}\,4\lambda(\cos\phi_n-\lambda)\right\}$$

$$\times\,p(\phi_n)\,d\phi_n \tag{9}$$

3. Suppressed Carrier (No Interleaving). When the carrier synchronization loop used to track the input phase is of the suppressed carrier type (e.g., a Costas loop), then the results of Section B.1 have to be somewhat modified since the appropriate domain for ϕ is no longer $(-\pi,\pi)$. In fact, for suppressed carrier tracking of BPSK with a Costas-type loop, and assuming perfect phase ambiguity resolution, ϕ takes on values only in the interval $(-\pi/2,\pi/2)$ [2]. Thus, the interval of integration for the first integral in Eq. (6) becomes $(-\pi/2,\pi/2)$ and the second integral in Eq. (6) disappears, i.e.,

$$E_\phi\{P(\underline{x}\to\hat{\underline{x}}\,|\,\phi;\lambda)\} =$$

$$\int_{-\pi/M}^{\pi/M}\frac{1}{2}\exp\left\{-\frac{E_s}{N_0}\,4\lambda(\cos\phi-\lambda)\,d_H(\underline{x},\hat{\underline{x}})\right\}p(\phi)\,d\phi \tag{10}$$

The significance of the second integral in Eq. (6) being equal to zero will be mentioned shortly relative to a discussion of *irreducible error probability*.

4. Suppressed Carrier (With Interleaving). Once again assuming suppressed carrier tracking of BPSK with a Costas-type

[3] Herein, for simplicity of notation, we drop the dependence of d_H on $\underline{x}$ and $\hat{\underline{x}}$.

loop, and perfect phase ambiguity resolution, one obtains, analogous to Eq. (9),[4]

$$E_\phi\left\{P(\underline{x}\to\underline{\hat{x}}\,|\phi;\lambda)\right\} = \frac{1}{2}\prod_{n=1}^{d_H}\int_{-\pi/2}^{\pi/2}\exp\left\{-\frac{E_s}{N_0}4\lambda(\cos\phi_n-\lambda)\right\}p(\phi_n)\,d\phi_n \tag{11}$$

III. Carrier Synchronization Loop Statistical Model and Average Pairwise Error Probability Evaluation

To evaluate Eq. (5), using Eqs. (6), (9), (10), or (11), one must specify the functional form of the probability density function (p.d.f.) $p(\phi)$ of the modulo 2π reduced phase error ϕ. For a discrete carrier synchronization loop of the phase-locked type, $p(\phi)$ is given by the Tikhonov p.d.f. [2]

$$p(\phi) = \begin{cases}\dfrac{\exp(\rho\cos\phi)}{2\pi I_0(\rho)}; & |\phi|\leqslant\pi\\ 0; & \text{otherwise}\end{cases} \tag{12}$$

where ρ is the SNR in the loop bandwidth.

In order to allow evaluation of Eq. (5) in closed form, one must recognize that for the case of no interleaving, Eq. (6) can be further upper bounded by using $(-\pi, \pi)$ instead of $(-\pi/2, \pi/2)$ in the first integral. Then, making this replacement

$$\min_\lambda E_\phi\left\{P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \min_\lambda\left(\frac{1}{2}\exp\left\{4d_H\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_A)}{I_0(\rho)}+I\right) \tag{13}$$

$$\rho_A \triangleq \rho - 4d_H\lambda\frac{E_s}{N_0}$$

$$I = \frac{1}{\pi I_0(\rho)}\left[\int_{\pi/2}^{\pi}\exp(\rho\cos\phi)\,d\phi\right]$$

[4]Note that the factor of 1/2 can be included here since for $0 \leqslant |\phi_n| \leqslant \pi/2$; $n\in\eta$, the condition on the first line of Eq. (7) is always satisfied and thus we need not use the looser upper bound of Eq. (8).

When Eq. (13) is substituted into Eq. (5), the term I will contribute an *irreducible error probability*, i.e., the system will exhibit a finite error probability when ρ is held fixed and E_s/N_0 approaches infinity. An example of such a system is one which apportions a fixed amount of the total available input power to a discrete carrier component for the purpose of deriving a coherent carrier reference at the receiver.

When interleaving is employed, Eq. (9) (minimized over λ) together with Eq. (12) become

$$\min_\lambda E_\phi\left\{P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \min_\lambda\left\{\prod_{n\in\eta}\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_B)}{I_0(\rho)}\right\} = \min_\lambda\left\{\left(\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_B)}{I_0(\rho)}\right)^{d_H}\right\} \tag{14}$$

$$\rho_B \triangleq \rho - 4\lambda\frac{E_s}{N_0}$$

For suppressed carrier tracking with a biphase Costas loop, $p(\phi)$ again has a Tikhonov-type p.d.f., which is given by [2] as

$$p(\phi) = \begin{cases}\dfrac{\exp(\rho\cos 2\phi)}{\pi I_0(\rho)}; & |\phi|\leqslant\dfrac{\pi}{2}\\ 0; & \text{otherwise}\end{cases} \tag{15}$$

Here ρ is the "effective" loop SNR which includes the effects of $S\times S$, $S\times N$, and $N\times N$ degradations commonly referred to as "squaring loss." Since suppressed carrier systems of this type derive their carrier demodulation reference from the data-bearing signal, the loop SNR, ρ, is directly proportional to E_s/N_0; thus there can be no irreducible error probability since $\rho\to\infty$ when $E_s/N_0\to\infty$. Furthermore, for perfect phase ambiguity resolution, it has been shown previously that for no interleaving, the term I is identically zero since the p.d.f. is zero in the region $(\pi/2, \pi)$. Thus, the average pairwise error probability results become

$$\min_\lambda E_\phi\left\{P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \min_\lambda\left\{\frac{1}{2}\exp\left\{4d_H\lambda^2\frac{E_s}{N_0}\right\}\frac{f_A(\rho)}{I_0(\rho)}\right\}$$

$$f_A(\rho) \triangleq \frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\exp\left\{\rho\cos 2\phi - 4d_H\lambda\frac{E_s}{N_0}\cos\phi\right\}d\phi \tag{16}$$

for no interleaving and

$$\min_{\lambda} E_{\phi}\left\{P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \min_{\lambda}\left\{\prod_{n\in\eta}\exp\left\{4\lambda^2\,\frac{E_s}{N_0}\right\}\frac{f_B(\rho)}{I_0(\rho)}\right\}$$

$$= \min_{\lambda}\left\{\left(\exp\left\{4\lambda^2\,\frac{E_s}{N_0}\right\}\frac{f_B(\rho)}{I_0(\rho)}\right)^{d_H}\right\}$$

$$f_B(\rho) \triangleq \frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\exp\left\{\rho\cos 2\phi - 4\lambda\,\frac{E_s}{N_0}\cos\phi\right\}d\phi \tag{17}$$

for the case of interleaving.

In arriving at Eqs. (13), (14), (16), and (17), we have assumed the "same type" of Chernoff bound in the sense that in all cases, the minimization over λ was performed *after* the averaging over ϕ. The principal reason for doing this is to allow comparison of performance with and without interleaving using bounds with "similar degrees of looseness." For the case of no interleaving, one can actually achieve a tighter bound than that given above by performing the minimization over λ on the conditional pairwise probability in Eq. (4). When this is done, one obtains

$$\lambda_{\text{opt}} = \frac{1}{2}\cos\phi \tag{18}$$

and Eq. (4) becomes

$$P(\underline{x}\to\underline{\hat{x}}\,|\phi) \leqslant \begin{cases}\frac{1}{2}\exp\left\{-\frac{E_s}{4N_0}\,d_H\cos^2\phi\right\}; & 0\leqslant|\phi|\leqslant\frac{\pi}{2}\\ 1; & \frac{\pi}{2}\leqslant|\phi|\leqslant\pi\end{cases} \tag{19}$$

Unfortunately, the integral of Eq. (19) over the p.d.f.s of Eqs. (12) and (15) cannot be obtained in closed form. Defining the integral

$$L(J) = \int_{-\pi/J}^{\pi/J}\exp\left\{-\frac{E_s d_H}{N_0}\cos^2\phi\right\}\frac{\exp(\rho\cos J\phi)}{\left(\frac{2\pi}{J}\right)I_0(\rho)}\,d\phi \tag{20}$$

then, the average pairwise error probabilities are now as follows:

Discrete Carrier

$$E_{\phi}\left\{\min_{\lambda} P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \frac{1}{2}L(1) + I \tag{21}$$

where I is defined in Eq. (13).

Suppressed Carrier

$$E_{\phi}\left\{\min_{\lambda} P(\underline{x}\to\underline{\hat{x}}\,|\underline{\phi};\lambda)\right\} \leqslant \frac{1}{2}L(2) \tag{22}$$

Using Eqs. (21) and (22) (rather than Eqs. 13 and 16) will result in a smaller improvement in performance due to interleaving/deinterleaving since Eqs. (21) and (22) result in a tighter bound on P_b (no interleaving).

IV. Evaluation of Bit Error Probability

A. Discrete Carrier Tracking

To evaluate the upper bound on bit error probability, e.g., Eq. (5), we use the transfer function bound approach [1], which, for the ideal case of perfect carrier synchronization, gives

$$P_b \leqslant \frac{1}{2}\frac{d}{dz}\,T(D,z)\Big|_{z=1} \tag{23}$$

where $T(D, z)$ is the transfer function of the pair-state diagram associated with the trellis diagram of the code. When noisy carrier synchronization references are present, the appropriate upper bound on bit error probability for the case of no interleaving becomes

$$P_b \leqslant \frac{1}{2}\left[2\int_0^{\pi/2}\frac{d}{dz}\,T(D(\phi),z)\Big|_{z=1}\,p(\phi)\,d\phi\right]$$

$$+ 2\int_{\pi/2}^{\pi}p(\phi)\,d\phi$$

$$= \int_0^{\pi/2}\frac{d}{dz}\,T(D(\phi),z)\Big|_{z=1}\,p(\phi)\,d\phi + I \tag{24}$$

where I is defined in Eq. (13) and from Eq. (19), the equivalent Bhattacharyya parameter becomes

$$D(\phi) = \exp\left\{-\frac{E_s}{N_0}\cos^2\phi\right\}; \qquad 0 \leqslant |\phi| \leqslant \frac{\pi}{2} \tag{25}$$

For the case of interleaving, we use Eq. (23) without the factor 1/2 and with D defined in accordance with Eq. (14), namely,

$$D = \min_{\lambda}\left(\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_B)}{I_0(\rho)}\right) \tag{26}$$

In arriving at Eq. (26), we have made use of the fact that, for any d,

$$\min_{\lambda}\left\{\left(\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_B)}{I_0(\rho)}\right)^d\right\} = \left\{\min_{\lambda}\left(\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{I_0(\rho_B)}{I_0(\rho)}\right)\right\}^d \tag{27}$$

Figures 2 through 10 illustrate the upper bound on bit error probability versus bit energy-to-noise ratio E_b/N_0 (E_b is related to E_s by $E_s = rE_b$ where r is the code rate) for the rate 1/2, constraint length 7 Voyager code, the rate 1/4, constraint length 15 Galileo experimental code [4], the rate 1/6, constraint length 15 "2 dB" code [5], and various values of loop SNR, ρ. In these curves we have assumed carrier synchronization with a PLL, i.e., the discrete carrier case.[5] On each figure are plotted the results for the case of no interleaving, the case of interleaving, and the case of no radio loss, i.e., ideal carrier synchronization. The transfer function bounds (truncated to 15 terms) on P_b for the above three codes are given in Table 1.

One may observe from the results in Figs. 2 through 10 that even for large values of ρ, e.g., 13 dB, a substantial reduction of bit error rate is possible by using interleaving. Also, since the tighter bound was used for the no-interleaving case and the looser bound for the interleaving case, the performance improvement illustrated is, as previously mentioned, somewhat pessimistic, i.e., in reality, one will do even better than shown.

[5] Also, in the computation of Eq. (24), we have set the value of one-half the derivative of the transfer function evaluated at $z = 1$ to one whenever it would normally exceed one. This is allowable since the conditional error probability cannot exceed one. Doing so results in a tighter bound.

B. Suppressed Carrier Tracking

The upper bound on bit error probability for the no-interleaving case is analogous to Eq. (23), and is given by

$$P_b \leqslant \int_0^{\pi/2}\frac{d}{dz}T(D(\phi),z)\bigg|_{z=1}p(\phi)\,d\phi \tag{28}$$

with $p(\phi)$ as in Eq. (15) and $D(\phi)$ as in Eq. (25). For the case of interleaving and the tighter upper bound, we again use Eq. (23) with, however, D now defined analogous to Eq. (26) by

$$D = \min_{\lambda}\left(\exp\left\{4\lambda^2\frac{E_s}{N_0}\right\}\frac{f_B(\rho)}{I_0(\rho)}\right) \tag{29}$$

where $f_B(\rho)$ is given in Eq. (17).

Assuming a Costas loop with integrate-and-dump arm filters (matched filters), the equivalent loop SNR is given by [2, 3]

$$\rho = \frac{1}{4}\left(\frac{S}{N_0B_L}\right)S_L = \frac{1}{4}\left(\frac{E_b}{N_0}\right)\left(\frac{1}{B_LT_b}\right)S_L; \qquad S_L = \frac{2\dfrac{E_s}{N_0}}{1+2\dfrac{E_s}{N_0}} \tag{30}$$

where S_L denotes the "squaring loss" associated with BPSK modulation. Figures 11 through 18 illustrate results analogous to Figs. 2 through 10 for the case of suppressed carrier tracking and various values of B_LT_b. Since, as already mentioned, in suppressed carrier systems there is no irreducible error (since, from Eq. (30), $\rho \to \infty$ as $E_b/N_0 \to \infty$), the noisy reference losses are much smaller to begin with (i.e., no interleaving) than for the discrete carrier case. Thus, for sufficiently small B_LT_b, interleaving does not provide significant improvement. We also observe from the above figures that the noisy reference losses are much larger for the rate 1/4 and rate 1/6 codes than for the rate 1/2 code. The reason for this is that for a given E_b/N_0, the value of E_s/N_0 is 3 dB smaller for the rate 1/4 code and 4.77 dB smaller for the rate 1/6 code than for the rate 1/2 code and thus, from Eq. (30), for the same value of B_LT_b, the equivalent loop SNR is smaller because of the increased squaring loss.

V. Concluding Remarks

It has been shown that by interleaving the transmitted coded bits in convolutionally coded systems the radio loss can be significantly reduced. The amount of this reduction depends on the particular convolutional code used and the region of operation of the system as characterized by such parameters as bit error rate and loop SNR. In some cases, the performance of the interleaved system is close to that of the ideal coherent detection case.

Acknowledgment

The authors would like to acknowledge Dr. F. Pollara for providing the entries of Table 1.

References

[1] A. J. Viterbi and J. K. Omura, *Principles of Digital Communication and Coding*, New York: McGraw-Hill, Inc., 1979.

[2] W. C. Lindsey and M. K. Simon, *Telecommunication Systems Engineering*, Englewood Cliffs, NJ: Prentice-Hall, Inc., 1973.

[3] J. H. Yuen, ed., *Deep Space Telecommunications Systems Engineering*, New York: Plenum Press, 1983.

[4] S. Dolinar, "A New Code for Galileo," *TDA Progress Report 42-93*, vol. January–March 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 83–96, May 15, 1988.

[5] J. H. Yuen and Q. Vo, "In Search of a 2-dB Coding Gain," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 26–33, November 15, 1988.

Table 1. Transfer function bounds of $r = 1/2$, $K = 7$, $r = 1/4$, $K = 15$, and $r = 1/6$, $K = 15$ convolutional codes

$$P_b \leq \frac{1}{2} \frac{d}{dz} T(D, z)\Big|_{z=1} = \frac{1}{2} \sum_{d=d_f}^{\infty} \beta_d D^d$$

$r = 1/2, K = 7$		$r = 1/4, K = 15$[a]		$r = 1/6, K = 15$	
d	β_d	d	β_d	d	β_d
10	36	35	6	56	2
11	0	36	2	57	15
12	211	37	16	58	2
13	0	38	8	59	0
14	1404	39	11	60	12
15	0	40	20	61	25
16	11633	41	24	62	56
17	0	42	76	63	43
18	77433	43	126	64	24
19	0	44	180	65	44
20	502690	45	255	66	62
21	0	46	416	67	48
22	3322763	47	628	68	62
23	0	48	850	69	167
24	21292910	49	1313	70	162

[a]This code has been incorporated as an experiment for the Galileo mission. It is a good code for a concatenated coding scheme but not the optimum code from the standpoint of maximizing d_f.

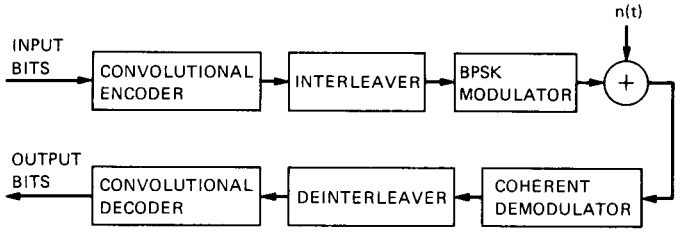


Fig. 1. System block diagram.

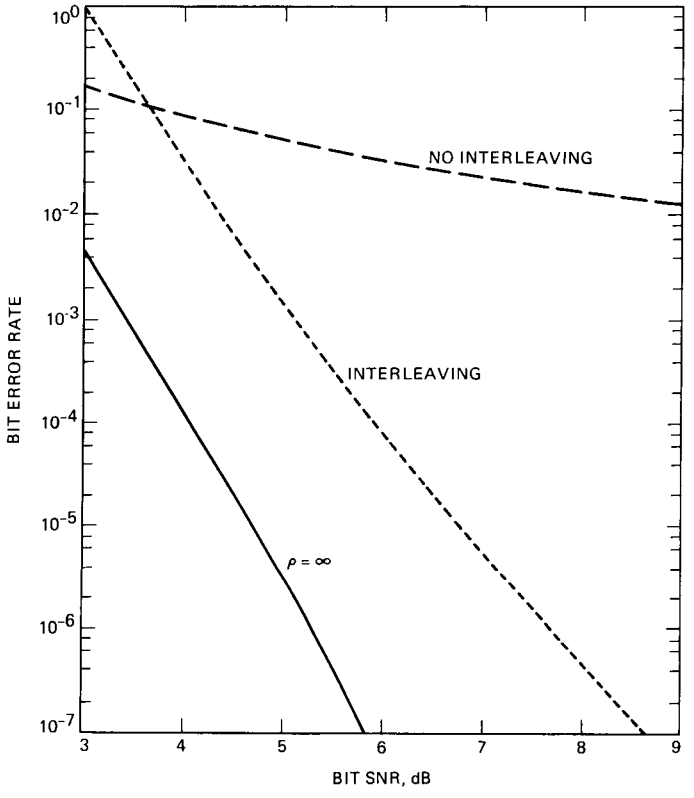


Fig. 2. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/2, constraint length 7 convolutional code; loop SNR = 7 dB; discrete carrier.

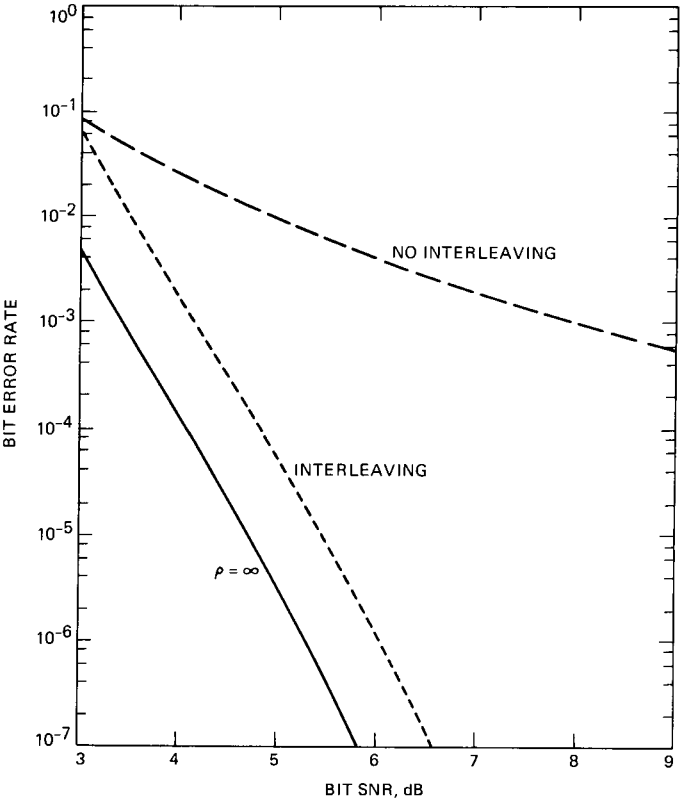


Fig. 3. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/2, constraint length 7 convolutional code; loop SNR = 10 dB; discrete carrier.

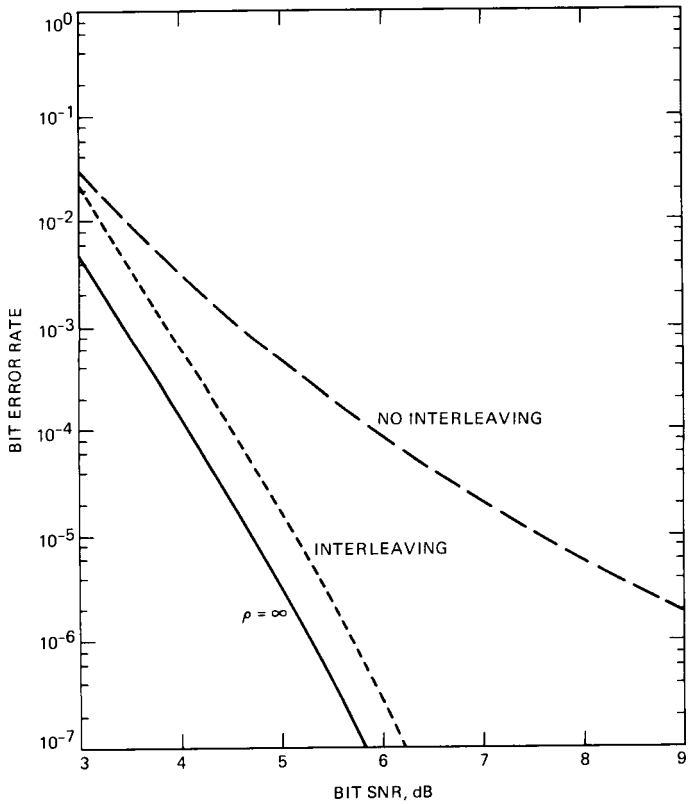


Fig. 4. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/2, constraint length 7 convolutional code; loop SNR = 13 dB; discrete carrier.

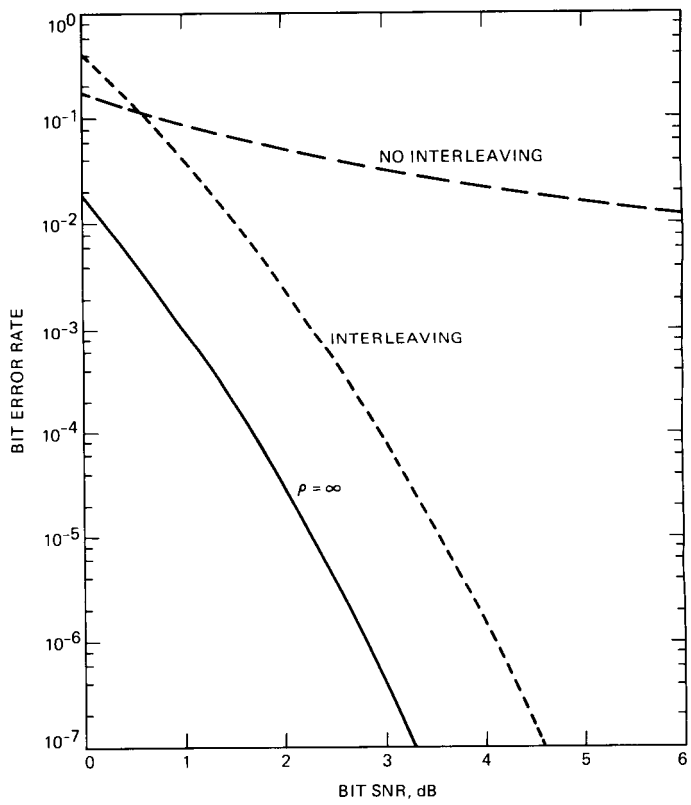


Fig. 5. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; loop SNR = 7 dB; discrete carrier.

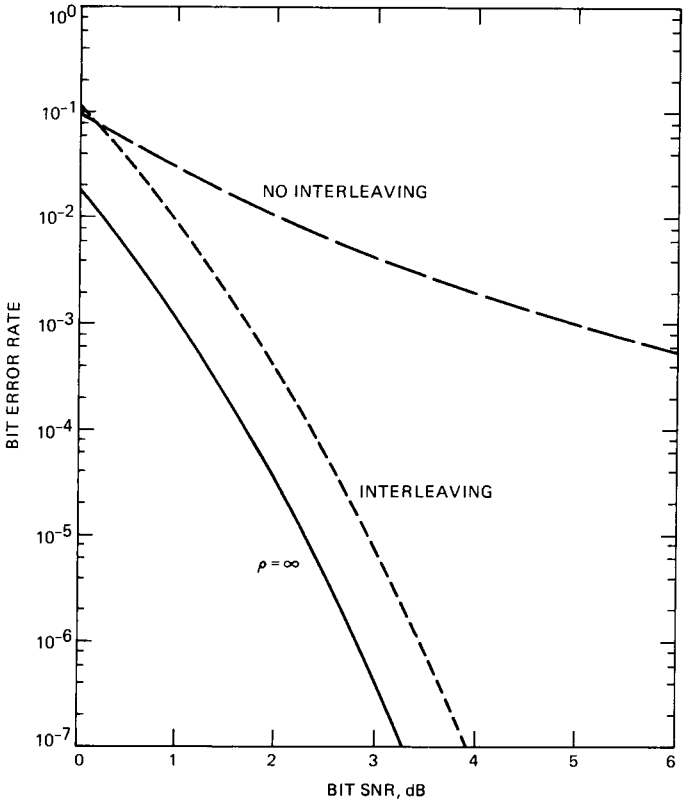


Fig. 6. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; loop SNR = 10 dB; discrete carrier.

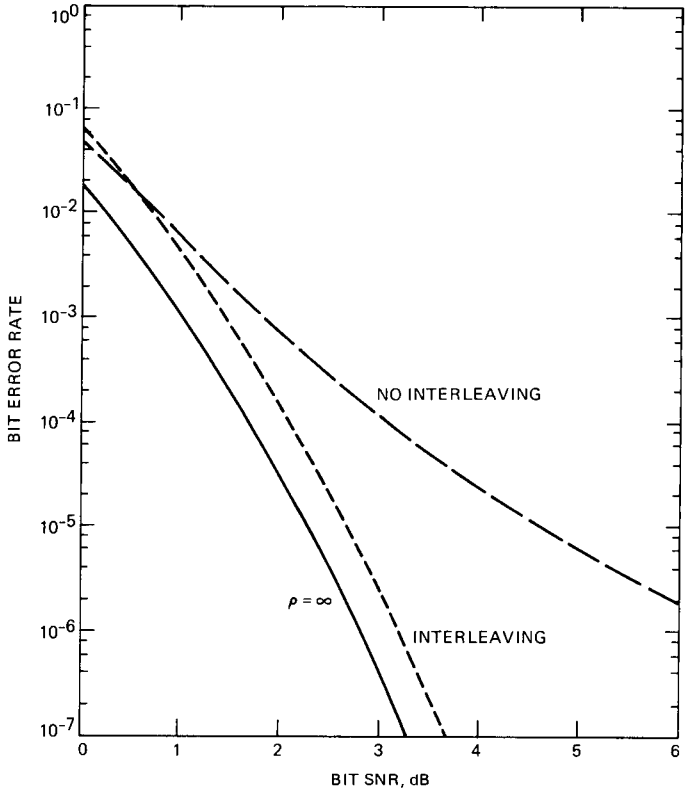


Fig. 7. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; loop SNR = 13 dB; discrete carrier.

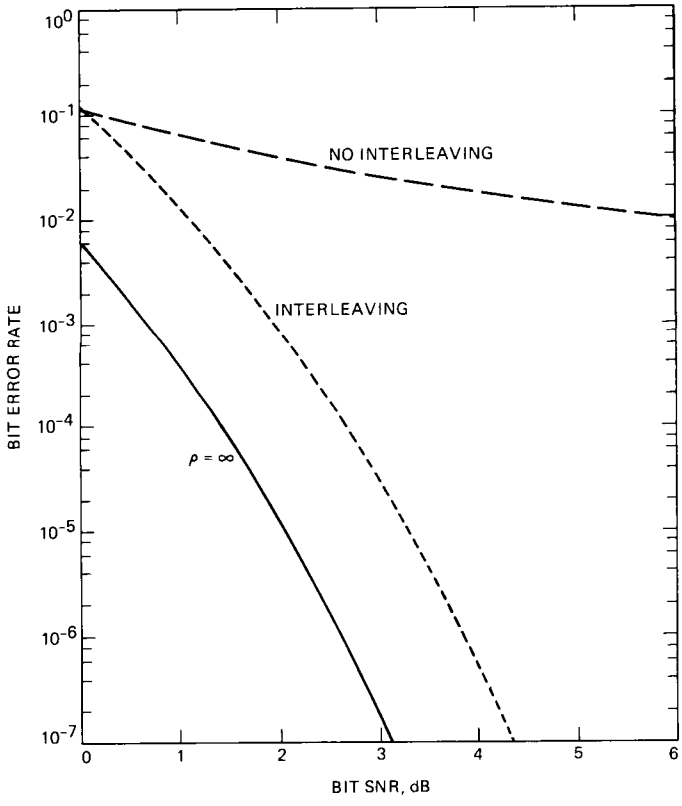


Fig. 8. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; loop SNR = 7 dB; discrete carrier.

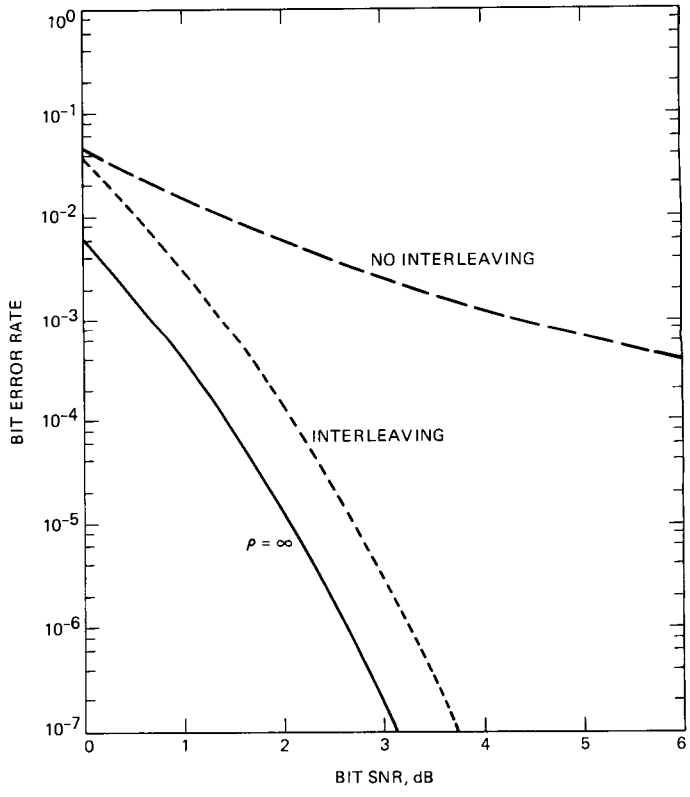


Fig. 9. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; loop SNR = 10 dB; discrete carrier.

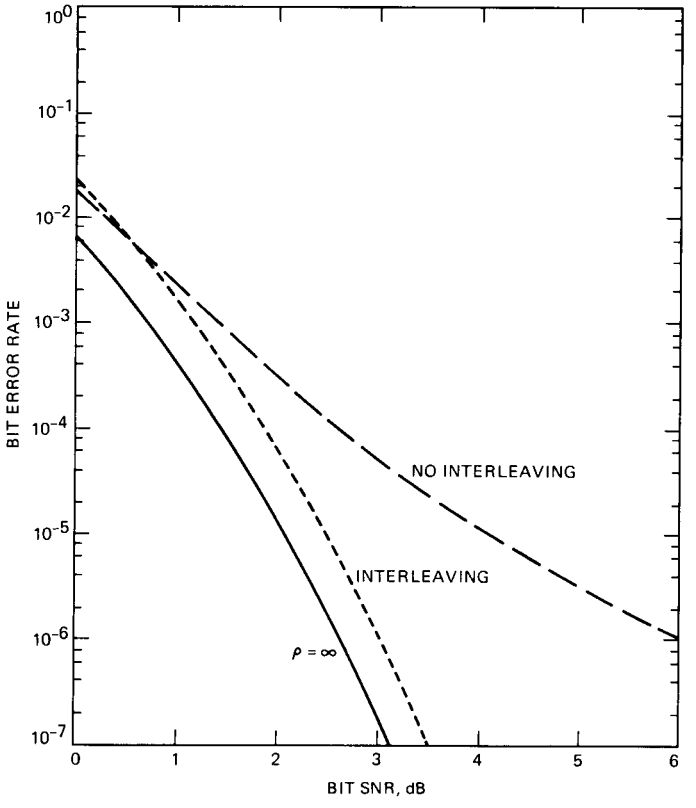


Fig. 10. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; loop SNR = 13 dB; discrete carrier.

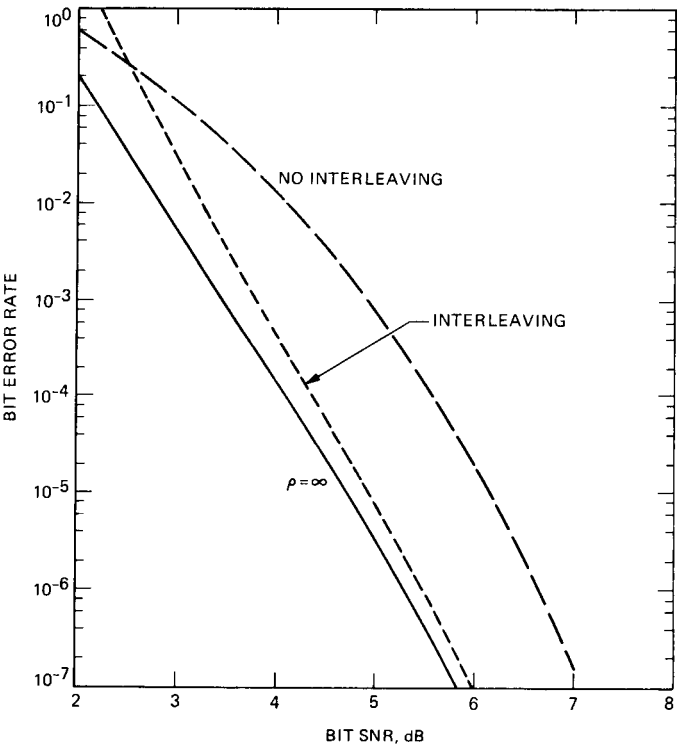


Fig. 11. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/2, constraint length 7 convolutional code; suppressed carrier; $1/B_L T_b = 10$.

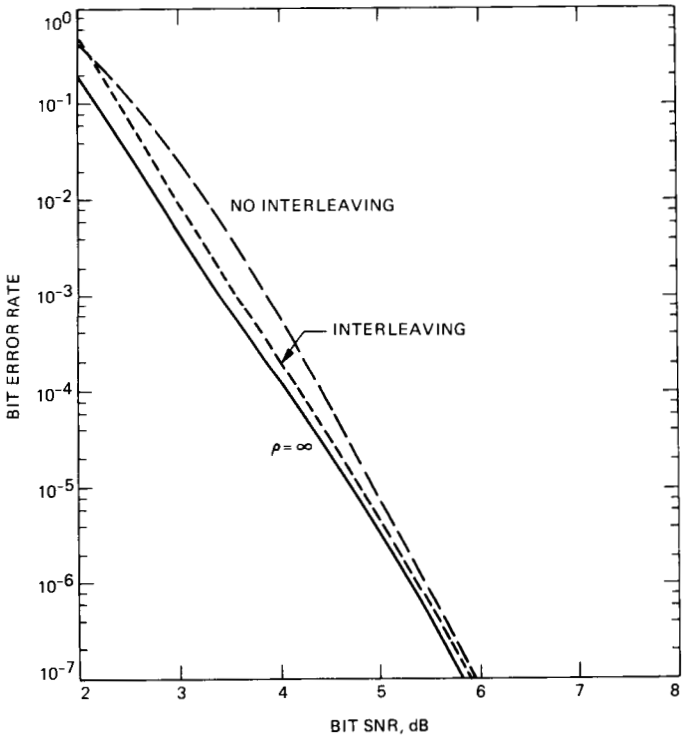


Fig. 12. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/2, constraint length 7 convolutional code; suppressed carrier; $1/B_L T_b = 20$.

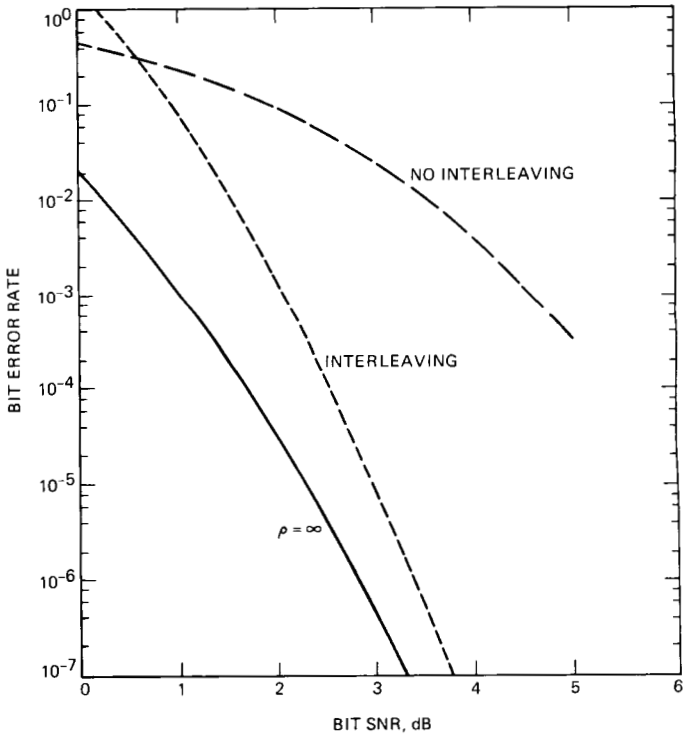


Fig. 13. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 10$.

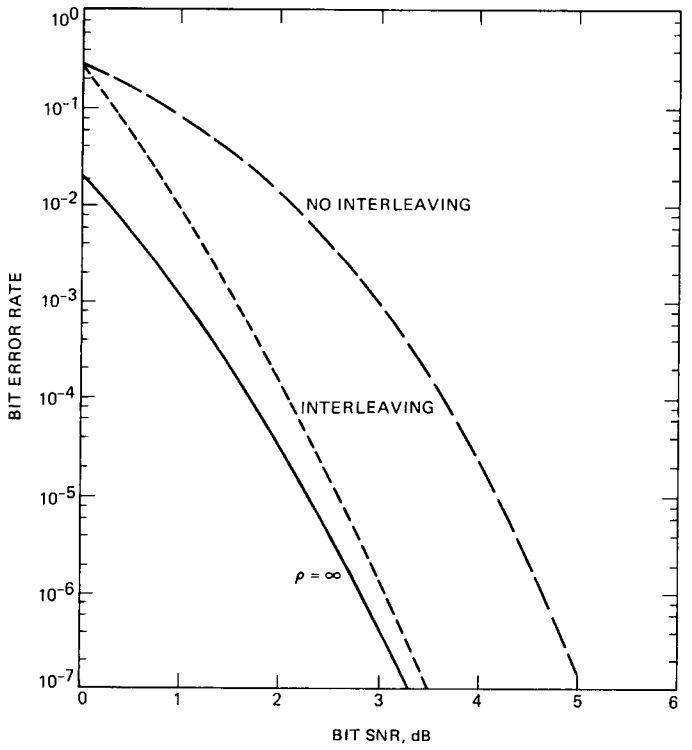


Fig. 14. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 20$.

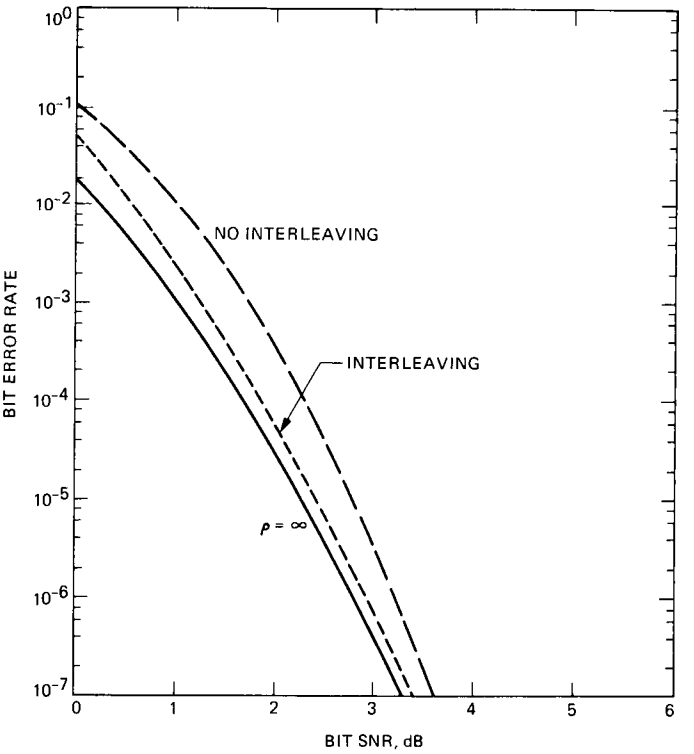


Fig. 15. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/4, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 40$.

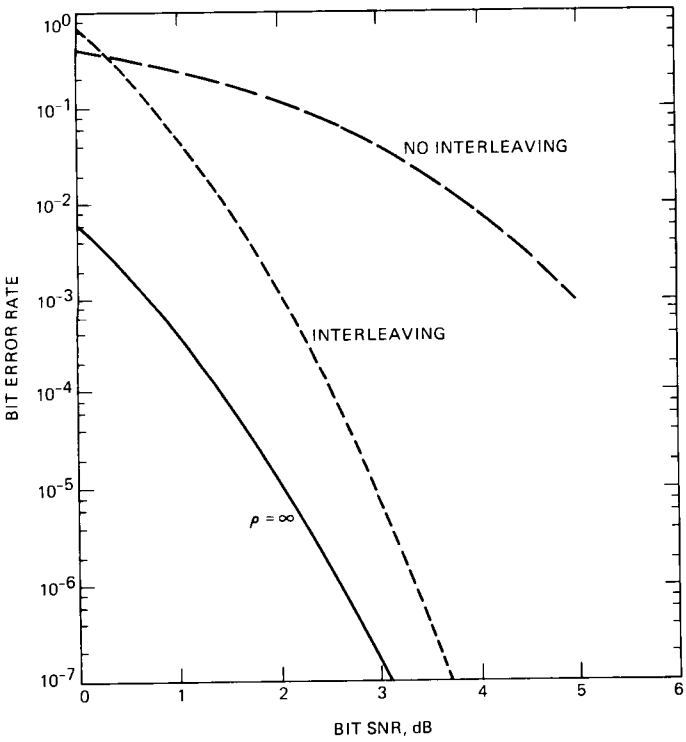


Fig. 16. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 10$.

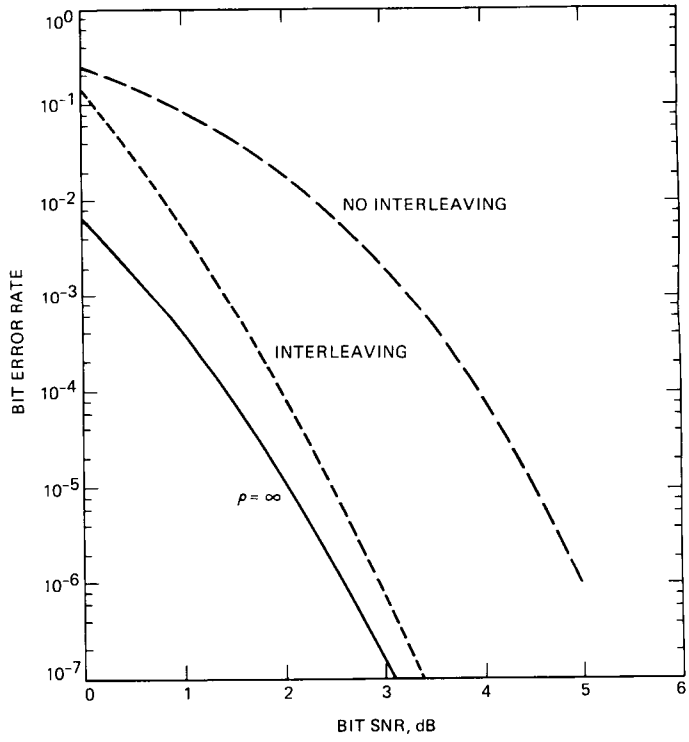


Fig. 17. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 20$.

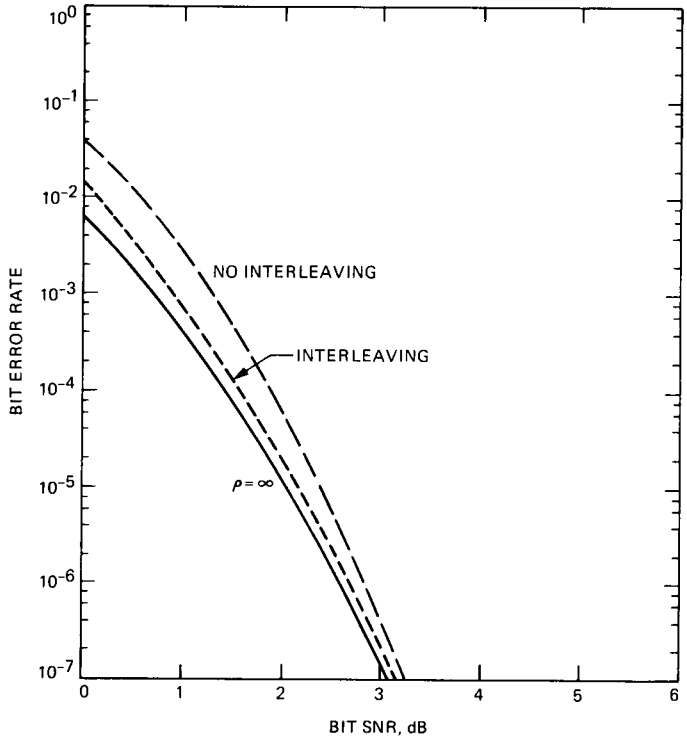


Fig. 18. Upper bound on average bit error probability versus bit energy-to-noise ratio for rate 1/6, constraint length 15 convolutional code; suppressed carrier; $1/B_L T_b = 60$.

Appendix

Derivation of an Upper Bound on the Pairwise Error Probability for Convolutionally Coded BPSK With Imperfect Carrier Phase Reference

Let $\underline{y} = (y_1, y_2, \ldots, y_N)$ denote the received sequence when the normalized (to unit power) sequence of MPSK symbols $\underline{x} = (x_1, x_2, \ldots, x_N)$ is transmitted. A *pairwise error* occurs if $\underline{\hat{x}} = (\hat{x}_1, \hat{x}_2, \ldots, \hat{x}_N) \neq \underline{x}$ is chosen by the receiver, which, if the receiver uses a distance metric to make this decision, implies $\underline{y}$ is closer to $\underline{\hat{x}}$ than to $\underline{x}$. Assuming that distance metric which is maximum-likelihood for ideal coherent detection (perfect carrier phase reference), then such an error occurs whenever

$$\sum_{n=1}^{N} \left| y_n - \hat{x}_n \right|^2 < \sum_{n=1}^{N} \left| y_n - x_n \right|^2 \tag{A-1}$$

Since BPSK is a constant envelope signaling set, we have $|x_n|^2 = |\hat{x}_n|^2 = 1$ (assuming a normalized signal) and Eq. (A-1) reduces to

$$\sum_{n=1}^{N} \mathrm{Re}\left\{ y_n \hat{x}_n^* \right\} > \sum_{n=1}^{N} \mathrm{Re}\left\{ y_n x_n^* \right\} \tag{A-2}$$

Letting n_n represent the additive noise in the nth signaling interval, and ϕ_n the phase shift introduced by imperfect carrier demodulation in that same interval, then y_n and x_n are related by

$$y_n = x_n e^{j\phi_n} + n_n; \qquad n = 1, 2, \ldots, N \tag{A-3}$$

Substituting Eq. (A-3) into Eq. (A-2) and simplifying gives

$$\mathrm{Re}\left\{ \sum_{n\in\eta} (\hat{x}_n - x_n)^* n_n \right\} > \mathrm{Re}\left\{ \sum_{n\in\eta} x_n (x_n - \hat{x}_n)^* e^{j\phi_n} \right\} \tag{A-4}$$

where η is the set of all n such that $x_n \neq \hat{x}_n$.

Since for an AWGN channel, n_n is a complex Gaussian random variable whose real and imaginary components have variance

$$E\left\{ [\mathrm{Re}(n_n)]^2 \right\} = E\left\{ [\mathrm{Im}(n_n)]^2 \right\} \triangleq \sigma^2 \tag{A-5}$$

then

$$\mathrm{var}\left\{ \mathrm{Re}\left\{ \sum_{n\in\eta} (\hat{x}_n - x_n)^* n_n \right\} \right\} = \sigma^2 \sum_{n\in\eta} \left| x_n - \hat{x}_n \right|^2 \tag{A-6}$$

and the conditional pairwise error probability $P(\underline{x} \to \underline{\hat{x}} \mid \underline{\phi})$ is given by

$$\begin{aligned} P(\underline{x} \to \underline{\hat{x}} \mid \underline{\phi}) &= \Pr\left\{ \mathrm{Re}\left\{ \sum_{n\in\eta} (\hat{x}_n - x_n)^* n_n \right\} \right. \\ &\quad \left. > \mathrm{Re}\left\{ \sum_{n\in\eta} x_n (x_n - \hat{x}_n)^* e^{j\phi_n} \right\} \right\} \\ &= Q\left\{ \frac{\mathrm{Re}\left\{ \sum_{n\in\eta} x_n (x_n - \hat{x}_n)^* e^{j\phi_n} \right\}}{\sigma \sqrt{\sum_{n\in\eta} \left| x_n - \hat{x}_n \right|^2}} \right\} \end{aligned} \tag{A-7}$$

where $\underline{\phi} = (\phi_1, \phi_2, \ldots, \phi_N)$ is the sequence of carrier phase errors and $Q(x)$ is the Gaussian integral defined by

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp\left(-\frac{y^2}{2} \right) dy \tag{A-8}$$

To simplify Eq. (A-7), proceed as follows. For BPSK modulation

$$\left| x_n - \hat{x}_n \right|^2 = 4; \qquad n \in \eta \tag{A-9}$$

and

$$\sum_{n\in\eta} \mathrm{Re}\left\{ x_n (x_n - \hat{x}_n)^* e^{j\phi_n} \right\} = 2 \sum_{n\in\eta} \cos\phi_n \tag{A-10}$$

Thus, Eq. (A-7) can be written as

$$P(\underline{x} \to \hat{\underline{x}} \mid \underline{\phi}) = Q\left(\frac{\sum_{n\in\eta} \cos\phi_n}{\sqrt{\sigma^2 d_H(\underline{x}, \hat{\underline{x}})}}\right) \tag{A-11}$$

where $d_H(\underline{x}, \hat{\underline{x}})$ is the Hamming distance between $\underline{x}$ and $\hat{\underline{x}}$, i.e., the number of elements in the set η (see Eq. 3).

The argument of the Gaussian integral in Eq. (A-11) is in the form $a/\sqrt{b}$. For $a > 0$, we can upper bound this integral by[1]

$$Q\left(\frac{a}{\sqrt{b}}\right) \leqslant \frac{1}{2} e^{-a^2/2b} \tag{A-12}$$

Since for any λ, we have $(a - 2\lambda b)^2 > 0$, rearranging this inequality gives the equivalent form

$$\frac{a^2}{b} \geqslant 4\lambda a - 4\lambda^2 b \tag{A-13}$$

[1]Note that for perfect carrier demodulation, i.e., $\phi = 0$, we always have $a > 0$.

Thus, for $a > 0$,

$$Q\left(\frac{a}{\sqrt{b}}\right) \leqslant \frac{1}{2} \exp\{-2\lambda [a - \lambda b]\} \tag{A-14}$$

For $a < 0$, the loose upper bound must be used

$$Q\left(\frac{a}{\sqrt{b}}\right) = Q\left(-\frac{|a|}{\sqrt{b}}\right) = 1 - Q\left(\frac{|a|}{\sqrt{b}}\right) \leqslant 1 \tag{A-15}$$

Finally, using Eqs. (A-14) and (A-15) in Eq. (A-11) gives the desired upper bound on pairwise error probability as

$$P(\underline{x} \to \hat{\underline{x}} \mid \underline{\phi}; \lambda) \leqslant$$

$$\begin{cases} \frac{1}{2} \exp\left\{-\frac{E_s}{N_0} \sum_{n\in\eta} 4\lambda(\cos\phi_n - \lambda)\right\}; & \sum_{n\in\eta} \cos\phi_n > 0 \\ 1; & \sum_{n\in\eta} \cos\phi_n \leqslant 0 \end{cases} \tag{A-16}$$

In Eq. (A-16), use is made of the fact that for the unnormalized system, $1/2\sigma^2 = E_s/N_0$ where E_s is the symbol energy and N_0 the noise spectral density, and λ is replaced by the normalized quantity $\lambda\sigma^2$. Also, note that if Eq. (A-16) is minimized over λ, then it is identically in the form of a Chernoff bound.

TDA Progress Report 42-96

October – December 1988

A New VLSI Architecture for a Single-Chip-Type Reed-Solomon Decoder

I. S. Hsu and T. K. Truong
Communications Systems Research Section

~~This article describes~~ a new very large scale integration (VLSI) architecture for implementing Reed-Solomon (RS) decoders that can correct both errors and erasures. This new architecture implements a Reed-Solomon decoder by using replication of a single VLSI chip. It is anticipated that this single-chip-type RS decoder approach will save substantial development and production costs. It is estimated that reduction in cost by a factor of four is possible with this new architecture. Furthermore, this Reed-Solomon decoder is programmable between 8-bit and 10-bit symbol sizes. Therefore, both an 8-bit CCSDS RS decoder and a 10-bit decoder are obtained at the same time, and when concatenated with a (15,1/6) Viterbi decoder, provide an additional 2.1-dB coding gain.

I. Introduction

A (255,223) 8-bit Reed-Solomon (RS) code in concatenation with a (7,1/2) Viterbi-decoded convolutional code has been recommended by the Consultative Commitee for Space Data Systems (CCSDS) as a standard coding system for the DSN downlink telemetry system [1]. Figure 1 shows a CCSDS-recommended DSN transmission system. This concatenated coding system, which is the so-called standard system, provides a coding gain of about 2 dB over the (7,1/2) Viterbi-decoded-only system. In Fig. 2, several curves representing performances of different coding schemes for the DSN are illustrated [2]. Recent software simulations show that a (1023,959) Reed-Solomon code, when concatenated with a (15,1/6) Viterbi-decoded convolutional code, provide another 2-dB coding gain over the standard system recommended by CCSDS [3]. This additional coding gain may be needed for future deep-space missions to save cost, since coding is among the most cost-efficient ways to improve system performance. A VLSI-based (15,1/6) Viterbi decoder is currently being developed at JPL to support the Galileo project and is expected to be operating by mid-1991 [4]. Therefore, a (1023,959) Reed-Solomon decoder is needed to provide the remainder of the 2-dB coding gain.

Recently, several VLSI architectures for implementing Reed-Solomon decoders have been proposed [5,6]. However, the complexity of a Reed-Solomon decoder increases with the symbol size of the code. It is very unlikely that current technology can implement a single-chip Reed-Solomon decoder that can correct both errors and erasures if the symbol size of the code is larger than 8 bits. The existing VLSI Reed-Solomon decoders use a natural scheme to partition the decoder system. In this natural partitioning scheme, as many functional blocks are grouped together as possible and realized on the same

VLSI chip. For example, the VLSI chip set developed by the University of Idaho has four different types of VLSI chips [6]. The first chip computes the syndromes. The second chip is the Euclid multiply/divide unit. The third chip performs as a polynomial solver. The final chip is the error-correction chip. This kind of partitioning scheme is straightforward. However, it is expected that several different types of VLSI chips are required to implement a Reed-Solomon decoder of symbol size larger than 8 bits. The costs to design, fabricate, and test VLSI-based systems increase drastically with the number of different chip types used. The (255,223) error-correcting-only RS decoder developed by the University of Idaho [5] consists of four different types of VLSI chips. Assuming it takes eight workmonths to design and test a VLSI chip, which is a reasonable assumption for a VLSI chip of this complexity, four different chips require 32 workmonths to develop. Furthermore, assuming it costs $80,000 to fabricate a VLSI chip of this complexity, the total fabrication cost of four RS chips is $320,000. In contrast, a single-chip-type RS decoder system takes only eight workmonths to design and test, and costs $80,000. Based on the above analysis, a single-chip-type RS decoder system is expected to have a four-fold cost savings compared to RS decoder systems using conventional partition schemes.

As described above, the (255,223) 8-bit RS code has been recommended by the CCSDS as part of the standard coding scheme in the DSN telecommunication system. Software simulations show system performance improvement obtained by concatenating a (1023,959) 10-bit RS decoder with a (15,1/6) Viterbi-decoded convolutional code. Therefore, there are reasons for developing both 8-bit and 10-bit RS decoders for current and future uses, and it is desirable to realize an RS decoder that is switchable between 8-bit and 10-bit codes. The key to realizing such an RS decoder is the development of an 8-bit and 10-bit switchable finite-field multiplier, which is the most frequently used functional building block in an RS decoder.

This article describes the development of a single-chip-type Reed-Solomon decoder system that is switchable between 8-bit and 10-bit symbol sizes (although this architecture is switchable between any two symbol sizes). The VLSI architecture of this chip is described in considerable detail. The architecture is regular, simple, and expandable, and therefore relatively easy to implement and test. It is expected that RS decoder systems using this architecture will have a four-fold cost reduction compared to conventional implementation schemes.

A Reed-Solomon code is a subset of the Bose-Chaudhuri-Hocquenghem (BCH) code [7]. Therefore, a decoding technique for BCH codes can also be used to decode a Reed-Solomon code. While many schemes have been developed for decoding Reed-Solomon codes [7], the so-called "transform-domain" and "time-domain" approaches are used most frequently.

As described in [5], a transform-domain RS decoder is suitable for small symbol sizes such as 8-bit or less, while the time-domain technique is suitable for large codes such as 10-bit or more. Because of the constraints on 10-bit decoding, the time-domain approach is chosen for the design of an RS decoder which is switchable between 8 and 10 bits.

A time-domain decoding algorithm can be described in the following steps:

(1) Compute syndromes and calculate the erasure-locator polynomial.

(2) Compute the Forney syndromes.

(3) Determine the errata-locator polynomial and the errata-evaluator polynomial by applying the Euclidean algorithm.

(4) Compute the errata locations by Chien search and compute the errata values.

(5) Perform the errata corrections.

Figure 3 shows a block diagram of a time-domain RS decoder; see [5] for more details.

In Section II, the VLSI design of a programmable finite-field multiplier is described. The VLSI architecture of the single-chip-type Reed-Solomon decoder is illustrated in Section III. Finally, concluding remarks are given in Section IV.

II. The Design of a Programmable Finite-Field Multiplier

The key element in the development of a programmable 8-bit and 10-bit switchable Reed-Solomon decoder is to design an 8-bit and 10-bit programmable finite-field multiplier. Finite-field multipliers are the basic building blocks in implementing a Reed-Solomon decoder. A comparison of VLSI architectures of finite-field multipliers using dual, normal, or standard bases is discussed in [8]. Since any finite-field element can be transformed into a standard-basis representation irrespective of its original basis, this article focuses on the programmable design of a standard-basis finite-field multiplier.

Figure 4 illustrates a logic diagram of a finite-field multiplier [9]. A mathematical theory for this finite-field-multiplier architecture is described as follows [9]:

Assuming the two inputs of the multiplier are $A = \alpha^i$ and $B = \alpha^j$, respectively, where α is a primitive element of $GF(2^m)$, then A and B can be represented as

$$A = \sum_{i=0}^{m-1} a_i \alpha^i$$

$$B = \sum_{i=0}^{m-1} b_i \alpha^i$$

The product of A and B, i.e., $C = \alpha^k$, can be represented as

$$C = \sum_{i=0}^{m-1} c_i \alpha^i$$

By the use of Horner's rule, the product C can be written

$$C = AB = A \sum_{k=0}^{m-1} b_k \alpha^k$$

$$= (\ldots((Ab_{m-1}\alpha + Ab_{m-2})\alpha + Ab_{m-3})\alpha$$

$$+ \ldots Ab_1)\alpha + Ab_0$$

or

$$C^{(0)} = Ab_{m-1}$$

$$C^{(1)} = Ab_{m-1}\alpha + Ab_{m-2} = C^{(0)}\alpha + Ab_{m-2}$$

$$C^{(i)} = C^{(i-1)}\alpha + Ab_{m-1-i}$$

$$C = C^{(m-1)} = C^{(m-2)}\alpha + Ab_0$$

Figure 5 shows the block diagram of the 10-bit standard-basis finite-field multiplier. Its extension to higher fields is obvious and straightforward. As shown in Fig. 5, this multiplier consists of 10 identical cells with each cell containing three 1-bit registers, two AND gates, and two XOR gates. There are three inputs to this multiplier. In Fig. 5, A and B represent the multiplicand and multiplier, respectively. They are represented in the basis of $\{\alpha^9, \alpha^8, \alpha^7, \alpha^6, \alpha^5, \alpha^4, \alpha^3, \alpha^2, \alpha^1, 1\}$. Another input f in Fig. 5 is the irreducible primitive polynomial, $f(X)$, of the field. Let

$$f(X) = X^{10} + f_9X^9 + f_8X^8 + f_7X^7 + f_6X^6 + f_5X^5$$

$$+ f_4X^4 + f_3X^3 + f_2X^2 + f_1X^1 + f_0X^0$$

where $f_i \in GF(2)$. In real-world application, both A and f can be loaded into the A-register and the f-register, respectively, in either parallel or serial form. (Figure 5 shows serial form for the purpose of illustration.) However, B must come in bit-by-bit with b_9 first and b_0 last. Initially, the C-register is reset to zero. At the first clock time, $C^{(0)}$ as described above is obtained; at the second clock time, $C^{(1)}$ is obtained, and so on. After 10 clock cycles, the final product C is obtained in the C-register. It can then be shifted out either in parallel or serial form, depending on the application.

A programmable standard-basis finite-field multiplier can be easily obtained by modifying the architecture depicted in Fig. 5. Figure 6 shows an 8-bit and 10-bit programmable finite-field multiplier. When signal ET is low, representing an 8-bit version, gate G1 is off and gate G2 is on. Therefore, the feedback will be conducted at 8-bit. Of course, all three inputs to the finite-field multiplier must reformat their representation. The highest two bits, i.e., a_9, a_8, b_9, b_8, f_9, and f_8, are all set equal to zero for 8-bit operation.

III. Architecture of the Single-Chip-Type Reed-Solomon Decoder System

A. VLSI Architecture of a Single-Chip-Type Reed-Solomon Decoder

This section describes the VLSI architecture of a single-chip-type Reed-Solomon decoder. The development of this new architecture is based on the VLSI architecture of an RS decoder described in [5]. Because of the regularity of a time-domain RS decoder structure, the functional units in an RS decoder can be efficiently partitioned. Figure 7 shows the architecture of a VLSI chip that is a basic building block of the single-chip-type Reed-Solomon decoder system. As shown in Fig. 7, the VLSI chip is partitioned into six rows. The first row of the chip consists of eight identical syndrome subcells. The 8-bit or 10-bit RS decoder is realized by making both the shift registers and the finite-field multipliers in all the subcells programmable between 8-bit and 10-bit operation.

The second row of the chip has eight polynomial expansion subcells; the third row consists of eight power expansion subcells. The fourth row of the chip has eight polynomial evaluation subcells which can also be used to do the Chien search operation. The fifth row has eight modified Euclidean subcells. Finally, the sixth row of the VLSI chip contains some miscel-

laneous cells such as counters, shift registers, finite-field multipliers and so forth. These miscellaneous cells are used as glue logic in a VLSI RS decoder system. As shown in Fig. 8, if four of these VLSI chips are connected in an array, a (255,223) time-domain RS decoder is formed since there are enough subcells to implement all the functional units. In other words, there are 32 syndrome subcells, 32 polynomial expansion subcells, 32 power expansion subcells, 32 polynomial evaluation/Chien search subcells, and 32 modified Euclidean algorithm subcells. Since all the subcells are programmable between 8-bit and 10-bit, the core of a 10-bit (1023,959) RS decoder is formed by arraying eight copies of this VLSI chip.

It is estimated that the total number of pins required for a VLSI chip is less than 132 and the total number of transistors per chip is less than 60,000. Obviously, these requirements are within today's VLSI technology capability.

The number of subcells in a VLSI chip could be reduced by half to decrease the silicon real estate and therefore increase chip yield. That is, only four subcells in each functional unit would be implemented on a VLSI chip. The number of transistors is reduced from 60,000 to 30,000 by this arrangement. On the other hand, if good fabrication technology is available, the number of functional subcells in a chip could be doubled such that the chip count in an RS decoder system is reduced by half. Therefore, this RS decoder architecture provides the maximum flexibility in both the chip and system designs.

B. Configuration of a Single-Chip-Type RS Decoder System

The system configuration of the proposed Reed-Solomon decoder is depicted in Fig. 9. As shown in Fig. 9, the system is partitioned into five units. There is a host computer (which could be a personal computer) to issue commands to the whole system. An input module which consists mostly of memory chips is used to store the received messages. Operations such as formatting, basis conversion if both standard and dual bases are used, zero-fill, etc., will be performed in this unit. Similarly, an output module is used to store the decoded symbols and perform operations such as basis reconversion, reformatting, and zero-stripping.

A control memory unit is used to store all the control signals for the VLSI chip. Due to the large number of control signals required for VLSI chips, it is not effective to include the control signal generation unit in the VLSI chip. The partitioning of the VLSI chip becomes very difficult if the control signal generators are included. It is expected that the control memory unit will consist of EPROMs which store control signals for the VLSI chip. Further modifications or expansions of control signals for the VLSI chip will be relatively easy in this scheme. Finally, the fifth part of the RS decoder system is the RS decoder VLSI chip set. This is the core of an RS decoder system.

IV. Conclusion

This article describes a new architecture for implementing a Reed-Solomon decoder. This new architecture uses a single-chip-type scheme that provides a minimum four-fold cost savings when compared to other RS decoder implementations. It is shown that a programmable finite-field multiplier will realize an 8-bit and 10-bit switchable RS decoder. The system configuration of an RS decoder is also described. An array of four identical VLSI chips forms an 8-bit CCSDS RS decoder and an array of eight identical VLSI chips forms a 10-bit RS decoder.

References

[1] "Recommendation for Space Data System Standards: Telemetry Channel Coding," (Blue Book), Consultative Committee for Space Data Systems, CCSDS Secretariat, Communications and Data Systems Division, Code TS, NASA, Washington, D.C., May 1984.

[2] R. L. Miller, L. J. Deutsch, and S. A. Butman, *On the Error Statistics of Viterbi Decoding and the Performance of Concatenated Codes*, JPL Publication 81-9, Jet Propulsion Laboratory, Pasadena, California, September 1, 1981.

[3] J. H. Yuen and Q. D. Vo, "In Search of a 2-dB Coding Gain," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 26–33, November 15, 1985.

[4] J. Statman, G. Zimmerman, F. Pollara, and O. Collins, "A Long Constraint Length VLSI Viterbi Decoder for the DSN," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 134–142, November 15, 1988.

[5] I. S. Hsu, T. K. Truong, I. S. Reed, L. J. Deutsch, and E. H. Satorius, "A Comparison of VLSI Architectures for Time and Transform Domain Decoding of Reed-Solomon Codes," *TDA Progress Report 42-92*, vol. October–December 1987, Jet Propulsion Laboratory, Pasadena, California, pp. 63–81, February 15, 1988.

[6] G. K. Maki, P. A. Owsley, K. B. Cameron, and J. Venbrux, "VLSI Reed-Solomon Decoder Design," *Proceedings of the Military Communications Conference (MILCOM)*, Monterey, California, pp. 46.5.1–46.5.6, October 5–9, 1986.

[7] R. E. Blahut, *Theory and Practice of Error Control Codes*, Reading, Massachusetts: Addison-Wesley, May 1984.

[8] I. S. Hsu, T. K. Truong, I. S. Reed, and L. J. Deutsch, "A Comparison of VLSI Architectures of Finite Field Multipliers Using Dual, Normal or Standard Bases," *IEEE Trans. on Computers*, vol. 37, no. 6, pp. 735–739, June 1988.

[9] P. A. Scott, S. E. Tavares, and L. E. Peppard, "A Fast VLSI Multiplier for $GF(2^m)$," *IEEE Journal on Selected Areas in Communications*, vol. SAC-4, no. 1, pp. 62–66, January 1986.

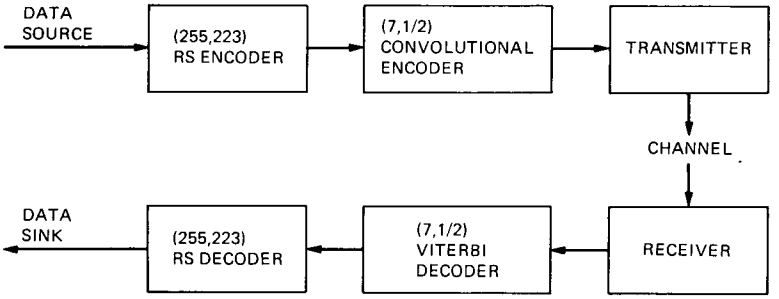


Fig. 1. Standard DSN telemetry coding system recommended by CCSDS.

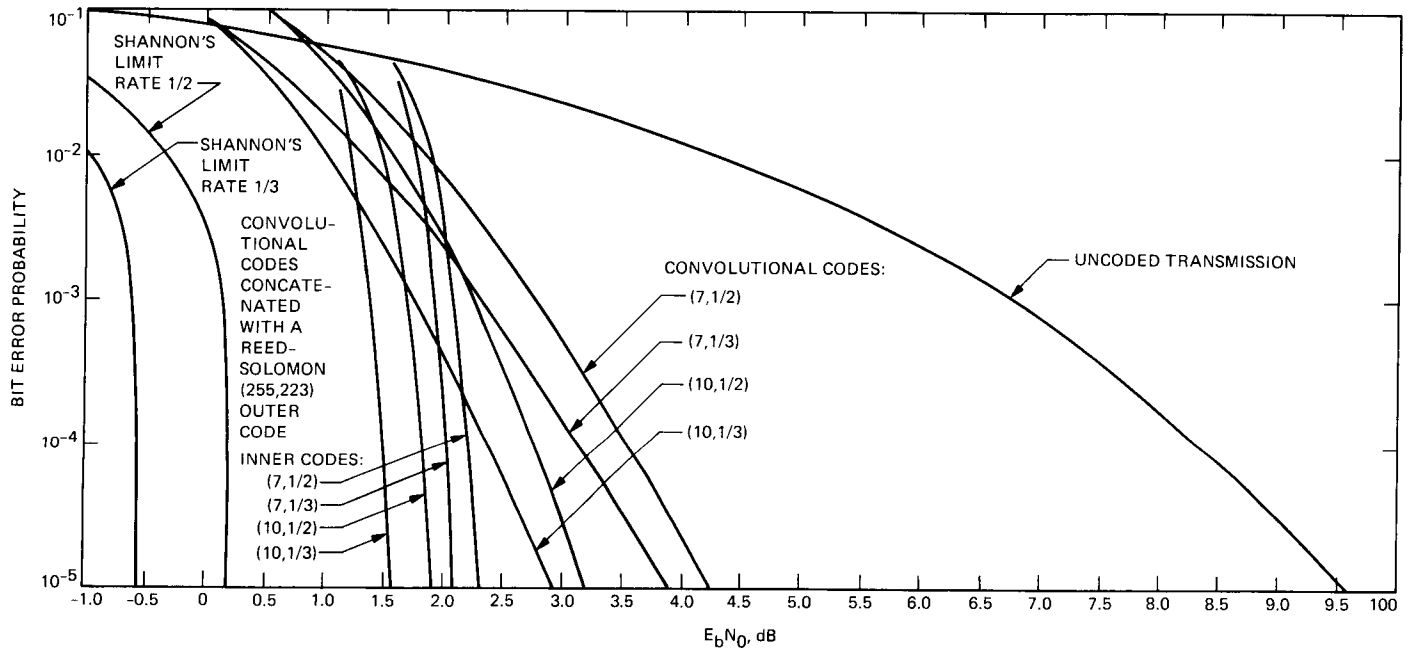


Fig. 2. Performance curves of various coding schemes in [2].

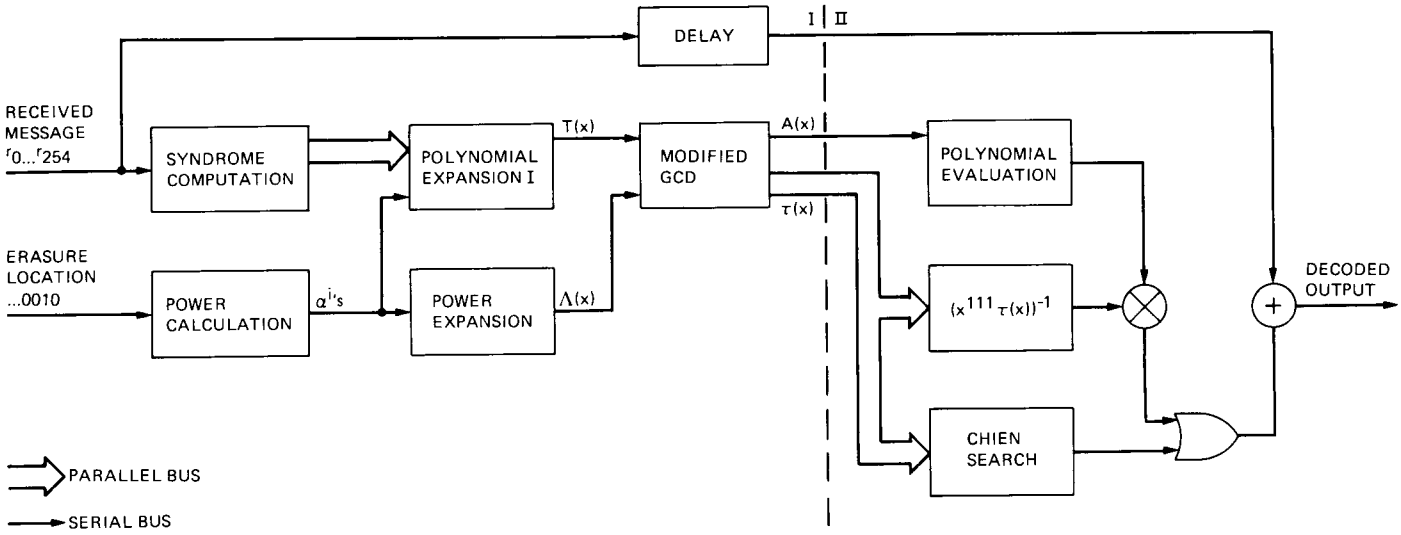


Fig. 3. Block diagram of a time-domain RS decoder for errors and erasures.

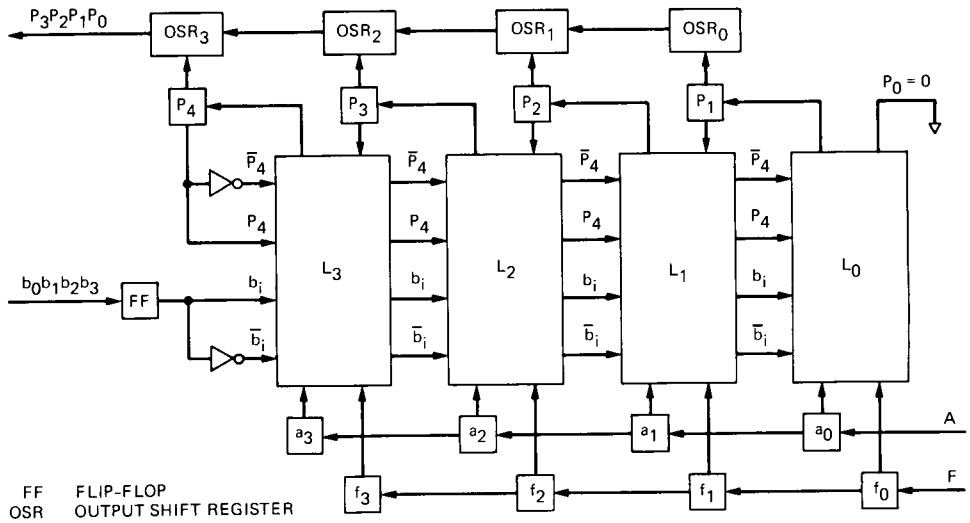


Fig. 4. Logic diagram of the standard-basis finite-field multiplier.

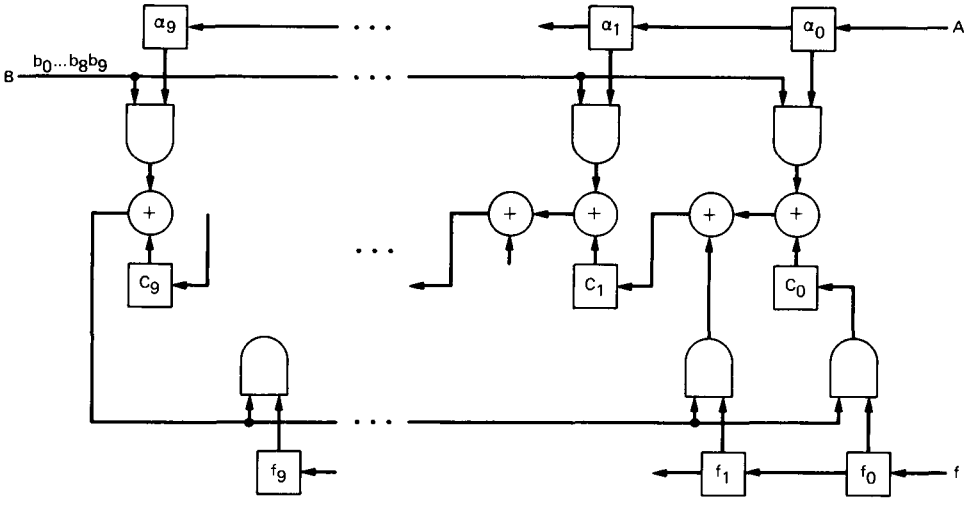


Fig. 5. Block diagram of a 10-bit standard-basis finite-field multiplier.

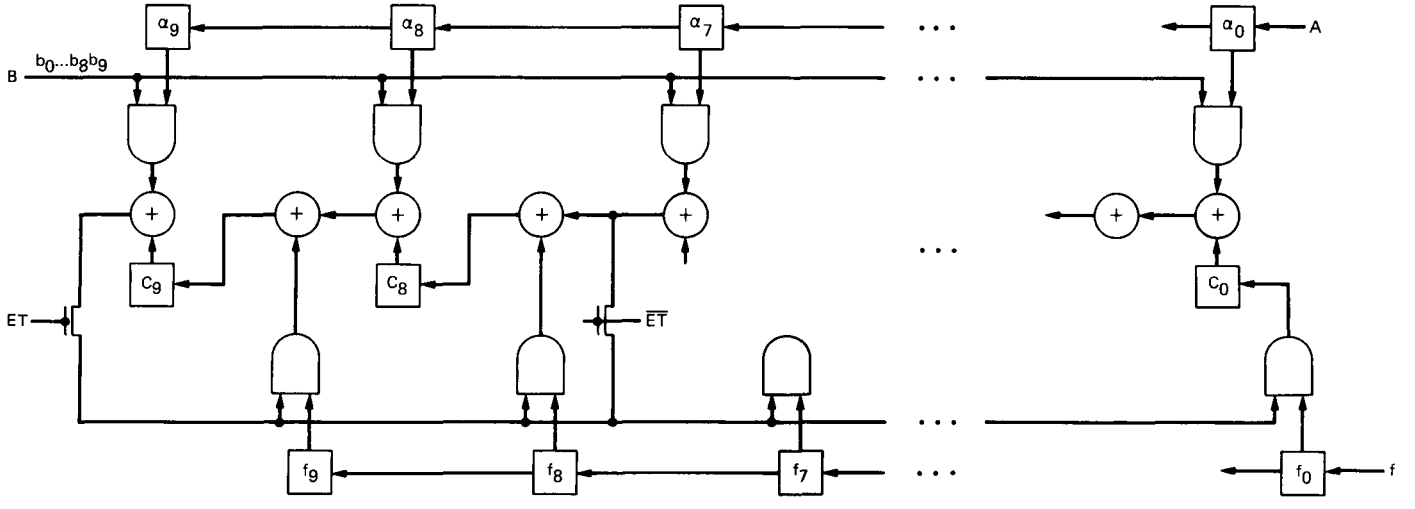


Fig. 6. Block diagram of an 8-bit and 10-bit switchable standard-basis finite-field multiplier.

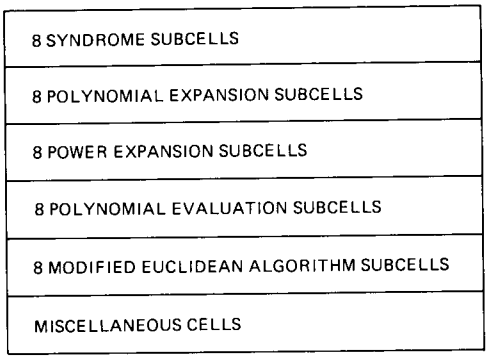


Fig. 7. Block diagram of VLSI chip architecture in the single-chip-type RS decoder system.

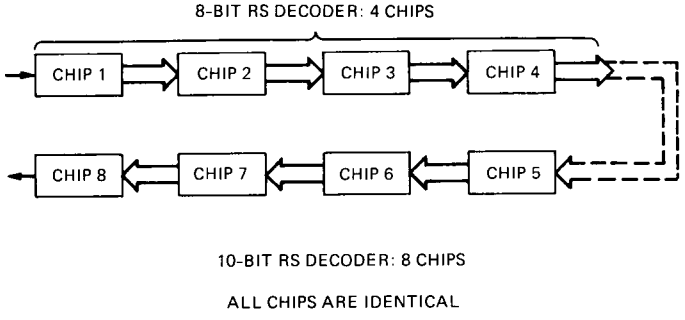


Fig. 8. Architecture of the 8-bit and 10-bit switchable RS decoder system.

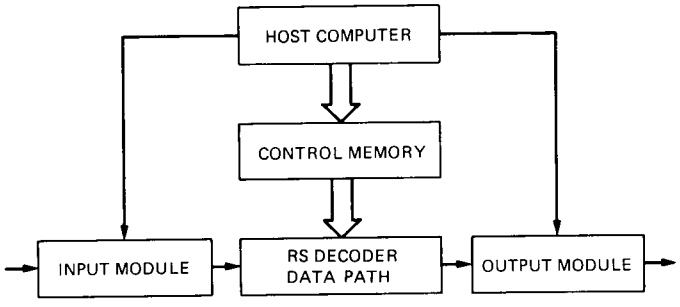


Fig. 9. Configuration of the proposed RS decoder system.

A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes

T. K. Truong and J. K. Holmes
Communications Systems Research Section

I. S. Reed and X. Yin
University of Southern California, Department of Electrical Engineering

In this article, a simplified procedure is developed to decode the three possible errors in a (23,12) Golay codeword. A computer simulation shows that this algorithm is modular, regular, and naturally suitable for both VLSI and software implementation. An extension of this new decoding procedure is used also to decode the 1/2-rate (24,12) Golay code, thereby correcting three and detecting four errors.

I. Introduction

The Golay code is a very useful code particularly for applications in which a parity bit is added to each codeword to yield a rate 1/2 code. The (24,12) Golay code is currently supported by the DSN. The 24-bit Golay code is also attractive for use on the DSN uplink where the spacecraft uses software decoding with the on-board computer. This code has been used on a number of communication links in the past, including the Voyager imaging system link.

This decoding problem originated with an investigation of the Digital Communication Terminal (DCT) communication link performance using the (23,12) Golay code. Coding analysts at JPL evaluated the properties of the Golay code, achieving a solution to the relatively simple decoding of the (23,12) and (24,12) Golay codes.

In the present article the BCH decoding algorithm described in [5] is extended to correct all three possible (correctable) errors of the code. This new decoding procedure is based on the fact that if one of the three errors in the block code of 23 digits can be canceled first, then the BCH decoding algorithm can be used to correct the remaining two errors.

This new Golay decoder is quite simple and similar to the Weldon decoding procedure [2]. One of the advantages of this algorithm over previous methods (see [1–3]) is that the new decoding algorithm is easily understood and readily implemented.

II. The (23,12) Binary Golay Code

It is not difficult to show that $\mathbf{g}(x) = x^{11} + x^9 + x^7 + x^6 + x^5 + x + 1$ is an irreducible polynomial over $GF(2)$. Thus, there exists an element $\alpha \in GF(2^{11})$ such that $\mathbf{g}(\alpha) = 0$. Hence, the elements of $GF(2^{11})$ are found in the following set:

$$GF(2^{11}) = \left\{ a_0 + a_1\,\alpha + a_2\,\alpha^2 + \ldots + a_{10}\,\alpha^{10} \mid a_0, a_1, \ldots, a_{10} \in GF(2) \right\} \quad (1)$$

Note also that α is a primitive twenty-third root of unity in $GF(2^{11})$. This fact shows that $\mathbf{g}(x)$ generates a cyclic BCH block code of length 23, called the Golay code.

The (23,12) Golay code is a perfect or close-packed code in the sense that the codewords and their 3-error correction spheres exhaust the vector space of 23-bit binary vectors. It is shown in [5] that the (23,12) Golay code is, besides being a cyclic BCH code, a quadratic-residue code. Since the minimum distance of the code is $d = 7$, one has the inequality $2t + 1 \leqslant d$, where t is the number of errors to be corrected. Hence the (23,12) Golay code allows for the correction of $t \leqslant 3$ errors.

The codewords of a Golay code over $GF(2)$ are expressed first as the coefficients of a polynomial. In such a representation a codeword is represented by

$$C(x) = \sum_{i=0}^{22} c_i x^i \tag{2}$$

where $c_i \in GF(2)$ and x is an indeterminant.

The generator polynomial of a Golay code as discussed above is an irreducible polynomial and given by

$$\mathbf{g}(x) = \prod_{i=0}^{10} (x - \alpha^{2^i})$$

$$= x^{11} + x^9 + x^7 + x^6 + x^5 + x + 1 \tag{3}$$

Now let polynomials

$$I(x) = c_{22}x^{22} + c_{21}x^{21} + \ldots + c_{11}x^{11} \tag{4}$$

and

$$P(x) = c_{10}x^{10} + c_9x^9 + \ldots + c_1x + c_0 \tag{5}$$

be the information and the parity-check polynomials of a codeword $C(x)$. Then the codeword in Eq. (2) is represented by

$$C(x) = I(x) + P(x) \tag{6}$$

To be a (23,12) cyclic BCH Golay codeword, $C(x)$ must also be a multiple of the generating polynomial $\mathbf{g}(x)$. That is,

$$C(x) = q(x)\mathbf{g}(x) \tag{7}$$

Polynomial $P(x)$ in Eq. (6) is obtained by dividing $I(x)$ by $\mathbf{g}(x)$, i.e.,

$$I(x) = q(x)\mathbf{g}(x) + \mathbf{r}(x) \tag{8}$$

where $\mathbf{r}(x)$ is a remainder polynomial of degree less than 11. Then one sets $P(x) = \mathbf{r}(x)$. Thus by Eqs. (6), (7), and (8) the following identities are true:

$$q(x)\mathbf{g}(x) = I(x) + \mathbf{r}(x) = I(x) + P(x) = C(x) \tag{9}$$

A code generated in this manner is a cyclic BCH code with parity check polynomial $P(x) = \mathbf{r}(x)$.

III. The Decoder for a (23, 12) Golay Code

A simple BCH decoding algorithm is developed in [5] to decode a (23,12) Golay code with only two or less errors. To illustrate this method, define

$$E(x) = e_{22}x^{22} + e_{21}x^{21} + \ldots + e_1x + e_0 \tag{10}$$

to be the error polynomial. Then the received codeword has the form

$$R(x) = C(x) + E(x) \tag{11}$$

Suppose that e errors occur in the received codeword $R(x)$ and assume that $2t \leqslant d - 1$. The decoder begins by dividing the received codeword $R(x)$ by the generator polynomial $\mathbf{g}(x)$. That is,

$$R(x) = V(x)\mathbf{g}(x) + S(x) \tag{12}$$

where $deg[S(x)] < deg[\mathbf{g}(x)]$ with $deg[\cdot]$ denoting degree of polynomial. Also by Eqs. (7) and (11),

$$R(x) = q(x)\mathbf{g}(x) + E(x) \tag{13}$$

Hence, by Eqs. (12) and (13) the syndrome polynomial $S(x)$ is found to be

$$S(x) = M(x)\mathbf{g}(x) + E(x) \tag{14}$$

where $M(x) = q(x) + V(x)$. Since α and α^3 are both roots of $\mathbf{g}(x)$, one has

$$s_1 \triangleq E(\alpha) = S(\alpha)$$

$$s_3 \triangleq E(\alpha^3) = S(\alpha^3) \tag{15}$$

where s_1 and s_3 are called the syndromes of the code.

The error-locator polynomial is defined by

$$\sigma(z) = \prod_{\beta = \text{error-locations}} (1 - \beta z) \tag{16}$$

For two errors, $\sigma(z)$ is given by the polynomial [5]

$$\sigma(z) = 1 + s_1 z + \left(s_1^2 + \frac{s_3}{s_1}\right) z^2 \tag{17}$$

where s_1 and s_3 are the syndromes defined in Eq. (15).

After reception, the 2-error correcting decoder computes by Eq. (15) the syndromes s_1 and s_3, as well as the error-locator polynomial given in Eq. (17). Depending on the number of errors, this BCH decoding algorithm (described in [5]) satisfies the following scheme:

$$\sigma(z) = \begin{cases} 1 & \text{if } s_1 = s_3 = 0, \text{ then no error} \\ 1 + s_1 z & \text{if } s_3 = s_1^3, \text{ then one error} \\ 1 + s_1 z + \left(s_1^2 + \dfrac{s_3}{s_1}\right) z^2 & \text{if } s_1 \neq 0 \text{ and } s_3 \neq 0, \text{ then two errors} \end{cases} \tag{18}$$

Note that the roots of $\sigma(z)$ are the inverse locations of the $t = 2$ errors.

From Eq. (18), it is evident that if there are no more than two errors, the errors can be located by the roots of $\sigma(z)$. Suppose $\sigma(z)$ does not have both its roots in the multiplicative subgroup of the field $GF(2^{11})$ consisting of the 23 roots of unity, namely, $\mathbf{G} = \{\alpha^i \mid 0 \leqslant i \leqslant 22\}$. Then this decoding procedure fails. Since a Golay code is perfect or close-packed, this implies that the above BCH decoding scheme in Eq. (18) detects more than two errors, namely, three errors.

IV. Decoder for Correcting Three Errors

For simplicity, let the transmitted error and received code be re-expressed, respectively, by the binary vectors: $\underline{c} = (c_0, c_1, c_2, \ldots, c_{22})$, $\underline{e} = (e_0, e_1, e_2, \ldots, e_{22})$ and $\underline{r} = (r_0, r_1, r_2, \ldots, r_{22})$.

Definition 1. Let the Hamming norm or weight of a binary vector $\underline{x} = (x_1, x_2, \ldots, x_n)$ be designated by $\|\underline{x}\|$. Then the set

$$\mathbf{T}_i \triangleq \{\underline{e} \mid \|\underline{e}\| = i\} \tag{19}$$

is the set of error vectors of weight i.

Definition 2. In terms of the Hamming norm or the weight, the Hamming distance between two vectors $\underline{x}$ and $\underline{y}$ is defined by

$$d(\mathbf{x},\mathbf{y}) \triangleq \|\mathbf{x} - \mathbf{y}\| \tag{20}$$

The above concepts are now used to prove the following theorem:

Theorem. Let $\underline{e}_4$ be any error vector of weight 4 and $\underline{c}$ be any code vector of the (23,12) Golay code. Then

$$\underline{x} \triangleq \underline{c} + \underline{e}_4 = \underline{c}_1 + \underline{e}_3 \tag{21}$$

where $\underline{c}_1$ is some other code vector and $\underline{e}_3$ is some error vector of weight 3. In other words, adding an error vector of Hamming weight 4 to a codeword of a Golay code produces a 23-bit vector which is equal to some other codeword plus an error vector of weight 3.

Proof: First, it is well known that the (23,12) Golay code is close-packed. That is, $\mathbf{B}_{23} = \mathbf{C}_0 \cup \mathbf{C}_1 \cup \mathbf{C}_2 \cup \mathbf{C}_3$ where $\cup$ denotes set union, $\mathbf{C}_0$ is the set of Golay code words, $\mathbf{B}_{23}$ is the set of all binary vectors of length 23 and

$$\mathbf{C}_i = \{\underline{x} \mid \underline{x} = \underline{c} + \underline{e}, \underline{c} \in \mathbf{C}_0, \underline{e} \in \mathbf{T}_i\} \qquad \text{for } i = 1, 2, 3$$

Hence, for any $\underline{c} \in \mathbf{C}_0$ and $\underline{e}_4 \in \mathbf{B}_{23}$, one has $\underline{x} = \underline{c} + \underline{e}_4 \in \mathbf{B}_{23}$, and $\underline{x} \notin \mathbf{C}_0$. Thus, by the close-packed nature of the code there exists $\underline{c}_1 \in \mathbf{C}_0$ and an error vector $\mathbf{e}$ such that

$$\underline{x} = \underline{c}_1 + \underline{e} \tag{22}$$

with

$$\|\underline{e}\| = \|\underline{x} + \underline{c}_1\| \leqslant 3 \tag{23}$$

Secondly, it is known that in a Golay code any nonzero codeword has a minimum weight of 7. Hence, by hypothesis and Eq. (22), one has the equalities

$$\|\underline{x} + \underline{c}_1\| = \|\underline{c}_1 + \underline{e}_4 + \underline{c}\| = \|\underline{e}\| \tag{24}$$

Also, since

$$\|\underline{x}+\underline{y}\| \geqslant \left|\|\underline{x}\| - \|\underline{y}\|\right| \qquad \text{and} \qquad \min_{\underline{c}_1 \neq \underline{c}} \|\underline{c}_1 + \underline{c}\| = 7$$

one has by Eq. (24) the inequalities

$$\|\underline{x}+\underline{c}_1\| = \|\underline{e}\| \geqslant \left|\|\underline{c}_1+\underline{c}\| - \|\underline{e}_4\|\right| \geqslant \left|7-4\right| = 3 \quad (25)$$

Thus by combining Eqs. (23) and (25), $\|\underline{e}\| = \|\underline{e}_3\| = 3$, and the theorem is proved. A geometric view of this proof is shown in Fig. 1.

Remark: The above theorem and its proof generalize to any close-packed error correcting code. However, since there is only one other nontrivial multiple error correcting perfect code, the (11,6) Golay code over $GF(3)$, such generality is somewhat academic.

Suppose the codeword $\underline{c} = (c_0, c_1, \ldots, c_{22})$ of the (23,12) Golay code is transmitted, and that the error vector $\underline{e} = (e_0, e_1, \ldots, e_{22})$ occurs with weight $t \leqslant 3$, where $d = 7 \geqslant 2t+1$. Also, let the received vector be

$$\underline{r} = \underline{c} + \underline{e} = (r_0, r_1, \ldots, r_{n-1}) \quad (26)$$

In this terminology, the new decoding method can be described as a recursive algorithm, as described below.

If $\underline{r}$ is corrupted by an error pattern $\underline{e}$ of weight $t \leqslant 2$, i.e., $\|\underline{e}\| \leqslant 2$, the BCH decoding method of Eq. (18) can correct all patterns of two or fewer errors. On the other hand, if the transmitted code $\underline{c}$ is corrupted by an error pattern $\underline{e}$ of weight three, i.e., $\|\underline{e}\| = 3$, then the scheme in Eq. (18) can be extended to correct three errors.

The first step in the decoding procedure is to cancel one error from $\underline{e}$. The second step is to correct the remaining two errors using the BCH method. To describe this algorithm, let $\underline{u}_1 = (1, 0, 0, \ldots, 0)$ be the "unit" 23-tuple vector. $\underline{u}_1$ has only one nonzero component, located at the first position. The sum of $\underline{r}$ and $\underline{u}_1$ is

$$\underline{r} + \underline{u}_1 = \underline{r}_1 = \underline{c} + \underline{e} + \underline{u}_1 \quad (27)$$

If one of the three errors in $\underline{e}$ is located at the first coordinate position, then $\|\underline{e} + \underline{u}_1\| = 2$, and the BCH decoding method for two errors in Eq. (18) can be used to correct the remaining two errors. However, if the first component of $\underline{e}$ is zero, then, by Theorem 1, $\underline{c} + \underline{e} + \underline{u}_1 = \underline{c}_1 + \underline{e}_1$, where $\|\underline{e}_1\| = 3$ and $\underline{c}_1 \in \mathbf{C}$ such that $\underline{c}_1 \neq \underline{c}$. In this case the BCH decoding method in Eq. (18) again can be used to detect the presence of three errors in received code vector $\underline{r}$.

Let ρ be the permutation which shifts the contents of the register right by one bit. Hence, a shift of $\underline{u}_1$ right by one bit is given by $\rho(\underline{u}_1) = \underline{u}_2 = (0, 1, 0, \ldots, 0)$. The sum of $\underline{r}_1$, $\underline{u}_1$, and $\underline{u}_2$ is given by

$$\underline{r}_2 = \underline{r}_1 + \underline{u}_1 + \underline{u}_2 = \underline{c} + \underline{e} + \underline{u}_2 \quad (28)$$

The same decoding procedure that was used on $\underline{r}_1$ is applied now to vector $\underline{r}_2$.

The procedure used above for the first and second coordinates of $\underline{r}$ is repeated recursively for at most 12 steps. For each step either one can correct all three errors or detect the fact that three errors still remain. Thus, if one shifts $\underline{u}_1$ through all of the information bits and one error is not canceled by the twelfth shift of $\underline{u}_1$, namely

$$\rho^{12}(\underline{u}_1) = (0,0,0,0,0,0,0,0,0,0,0,0,1,0,\ldots,0)$$

it is evident that all three errors exist only in the parity bits and therefore the information bits are not in error and can be decoded directly.

The overall decoding of a (23,12) Golay code is summarized by the following steps:

1. Apply the BCH procedure of Eq. (18) to decode the received 23-bit code vector $\underline{r}$. If an error vector $\underline{e}$ occurs with weight $t \leqslant 2$, i.e., $\|\underline{e}\| \leqslant 2$, the error pattern can be corrected. If $\|\underline{e}\| = 3$, the BCH procedure in Eq. (18) fails, but detects that three errors must corrupt vector $\underline{r}$.
2. Next, the first received information bit is inverted. Then the BCH procedure is applied again to the received code $\underline{r}$ now modified in the first bit. If $\|\underline{e}\| \leqslant 2$, the above inversion of the first bit corrects this bit. Thus the BCH method can now be used to correct the other two errors. On the other hand, if the first information bit was originally correct, the BCH method detects the fact that the three errors still remain in the codeword.
3. Repeat step 2 by inverting the second, third, ..., twelfth bits. If the BCH method still detects three errors with the received vector changed at the twelfth position, then all errors are confined to the parity check section.

Example: The following example illustrates how the decoding algorithm corrects 3 errors in one received codeword.

Encoding

Let $I(x)$ and $\mathbf{g}(x)$ be the information and generator polynomials. Then $P(x)$, the parity polynomial, is found by $P(x) = I(x) \bmod \mathbf{g}(x)$. That is,

$$I(x) = x^{22} + x^{20} + x^{18} + x^{17} + x^{15} + x^{14} + x^{12} + x^{11}$$

$$\mathbf{g}(x) = x^{11} + x^9 + x^7 + x^6 + x^5 + x + 1$$

$$P(x) = x^{10} + x^9 + x^7 + x^6 + x^5 + x^4 + x^3 + 1$$

Hence the codeword vector is

$$\underline{\mathbf{c}} = 1\,0\,1\,0\,1\,1\,0\,1\,1\,0\,1\,1 \quad 1\,1\,0\,1\,1\,1\,1\,1\,0\,0\,1$$

Channel-Noise

The three random errors are introduced at the 20th, 18th, and 9th bit of the codeword. Then the error pattern is given by

$$\underline{\mathbf{e}} = 0\,0\,1\,0\,1\,0\,0\,0\,0\,0\,0\,0 \quad 0\,1\,0\,0\,0\,0\,0\,0\,0\,0\,0$$

and the received codeword is

$$\underline{\mathbf{r}} = 1\,0\,0\,0\,0\,1\,0\,1\,1\,0\,1\,1 \quad 1\,0\,0\,1\,1\,1\,1\,1\,0\,0\,1$$

Decoding

Loop 1. First the syndrome $S(x)$ is found from codeword $R(x)$ by $R(x) \bmod \mathbf{g}(x)$. That is,

$$R(x) = x^{22} + x^{17} + x^{15} + x^{14} + x^{12} + x^{11} + x^{10} + x^7 + x^6 + x^5 + x^4 + x^3 + 1$$

$$S(x) = x^9 + x^7 + x^6 + x^5 + x^4 + x^3 + 1$$

$$s_1 = S(\alpha) = \alpha^9 + \alpha^7 + \alpha^6 + \alpha^5 + \alpha^4 + \alpha^3 + 1$$

$$s_3 = S(\alpha^3) = \alpha^9 + \alpha^8 + \alpha^7 + \alpha^6 + \alpha^3 + \alpha^2 + \alpha^1$$

$$s_1^3 = [S(\alpha)]^3 = \alpha^9 + \alpha^8 + \alpha^7 + \alpha^5 + \alpha^1$$

Since $s_1 \neq s_3 \neq 0$, $s_1^3 \neq s_3$, there are at least two errors. Thus,

$$\sigma(z) = 1 + s_1 z + \left(s_1^2 + \frac{s_3}{s_1}\right) z^2$$

Multiplying both sides by s_1 one has

$$\sigma'(z) = s_1 + s_1^2 z + \left(s_1^3 + s_3\right) z^2$$

Using the Chien search on $\sigma'(z)$, two roots cannot be found. Hence there are three errors.

Loop 2. Next invert the first bit of the received codeword. Use the same procedure as in Loop 1. Two roots still cannot be found.

Loop 3. Same as Loop 2, but invert the second bit.

Loop 4. After inverting the third bit, the syndrome polynomial and syndromes are given by

$$S(x) = x^{10} + x^6 + x^5 + x^3 + x^2$$

$$s_1 = S(\alpha) = \alpha^{10} + \alpha^6 + \alpha^5 + \alpha^3 + \alpha^2$$

$$s_3 = S(\alpha^3) = \alpha^8 + \alpha^4$$

Since $s_1^3 = \alpha^{10} + \alpha^8 + \alpha^3 + \alpha^2 + \alpha^1$, then $s_1 \neq s_3 \neq 0$ and $s_1^3 \neq s_3$. Thus one has for the error-locator polynomial

$$\sigma'(z) = (\alpha^{10} + \alpha^6 + \alpha^5 + \alpha^3 + \alpha^2) + (\alpha^{10} + \alpha^9 + \alpha^8 + \alpha^1 + \alpha^0) z + (\alpha^{10} + \alpha^4 + \alpha^3 + \alpha^2 + \alpha^1) z^2$$

From the Chien search, it is found that

$$\sigma'(\alpha^5) = (\alpha^{10} + \alpha^6 + \alpha^5 + \alpha^3 + \alpha^2) + (\alpha^{10} + \alpha^9 + \alpha^8 + \alpha^1 + \alpha^0)\alpha^5 + (\alpha^{10} + \alpha^4 + \alpha^3 + \alpha^1 + \alpha^0)\alpha^{10} = 0$$

$$\sigma'(\alpha^{14}) = (\alpha^{10} + \alpha^6 + \alpha^5 + \alpha^3 + \alpha^2) + (\alpha^{10} + \alpha^9 + \alpha^8 + \alpha^1 + \alpha^0)\alpha^{14} + (\alpha^{10} + \alpha^4 + \alpha^3 + \alpha^1 + \alpha^0)\alpha^{28} = 0$$

Hence, one has two roots, namely, $\beta_1 = \alpha^5$ and $\beta_2 = \alpha^{14}$. Thus all errors are located. Summarizing, one has

$$\text{first error position} = \alpha^{21}$$

$$\text{second error position} = \beta_1^{-1} = \alpha^{23-5} = \alpha^{18}$$

$$\text{third error position} = \beta_2^{-1} = \alpha^{23-14} = \alpha^{9}$$

After correctng the received codeword according to these error locations, the successfully decoded codeword is given by

$$\hat{\underline{c}} = 101011011011111011111001$$

The flowchart of this new algorithm is shown in Fig. 2. In a computer simulation, several hundred random codes with three or less errors were created and decoded perfectly with an average speed of 1.67 seconds per code. These results are shown in more detail in Table 1. The above algorithm is extended to the 1/2-rate (24,12) Golay code in the next section.

V. The (24, 12) Golay Code

A (24,12) Golay codeword can be formed by adding an even or odd parity-check bit to the (23,12) Golay codeword. It is shown easily that such a (24,12) Golay code has the minimum distance $d_{\min} = 8$. Thus, the new decoding algorithm for the extended (24,12) Golay code can be used to correct three or less errors and to detect the presence of four errors.

There is no loss in generality to assume that the parity of a (24,12) Golay codeword is even. That is, the sum of the 24 bits modulo 2 is equal to zero. Assume during transmission that four errors are added to the codeword. There are two cases to consider, as follows:

1. If the four errors occur in the first 23 bits, then by the theorem in Section IV, the addition of an error vector of Hamming weight 4 to a codeword produces a 23-bit vector which is equal to some other (23,12) Golay codeword plus an error vector of weight 3. Thus if the new decoding algorithm in Section IV is applied to the first 23 bits, an error vector of weight 3 is added to the received codeword. As a consequence, the parity of the (24,12) codeword also is changed. Hence, by checking the parity of the decoded codeword, the decoder detects the presence of four errors.
2. On the other hand, if three errors occur in the first 23 bits, and one error occurs in the parity bit, the new decoding algorithm corrects the three errors in the first 23 bits. The parity of the 23-bit decoded codeword now differs from the received parity bit. Hence, the decoder detects the presence of four errors.

The extended decoding algorithm for the (24,12) Golay code is summarized as follows: apply the simplified decoding algorithm to the first 23 bits. If the number of errors is less than 3, the decoding procedure terminates normally. If the number of errors is greater than or equal to 3, the parity of the decoded codeword is compared with the received parity bit. If they are different, the decoder detects four errors.

The detailed flowchart of the above decoding procedure is shown in Fig. 3. Finally, a comparison of the average computer times to decode the (23,12) and (24,12) Golay codes is given in Table 1. The decoding speeds for the (24,12) Golay codes are slightly lower due to the possibility of the parity bit being in error.

VI. Conclusion

An extended BCH algorithm is obtained for correcting three errors in a (23,12) Golay code. This procedure is based on the fact that if one bit is reversed in a codeword which has three errors, this codeword changes to another codeword which still has three errors. Hence, if one of the three errors can be canceled first, then the standard BCH decoding procedure can be used to correct the remaining two errors. A computer simulation shows that this procedure is very modular and naturally suitable for both software and VLSI implementation.

It is shown in the flowchart of Fig. 3 that the above new algorithm can be extended to decode the 1/2-rate (24,12) Golay code. The decoding algorithm for the (24,12) Golay code corrects 3 or less errors and detects the presence of 4 errors.

Acknowledgment

The authors wish to thank Mr. Rodney Pau at the University of Southern California for his help in computer programming.

References

[1] T. Kasami, "A Decoding Procedure for Multiple-Error-Correcting Cyclic Codes," *IEEE Trans. Information Theory*, IT-10, pp. 134–139, April 1964.

[2] S. Lin and D. J. Costello, Jr., *Error Control Coding: Fundamentals and Applications*, New Jersey: Prentice-Hall, Inc., 1983.

[3] F. J. MacWilliams, "Permutation Decoding of Systematic Codes," *Bell Syst. Tech. J.*, vol. 43, part 1, pp. 485–505, January 1964.

[4] F. J. MacWilliams and W. J. A. Sloane, *The Theory of Error-Correcting Codes*, Amsterdam: North-Holland, 1977.

[5] E. R. Berlekamp, *Algebraic Coding Theory*, New York: McGraw-Hill, 1968.

Table 1. *The computer time needed for decoding*

Number of errors	Average computer CPU time, sec
0	0.001
1	0.173
2	0.232
3	1.67

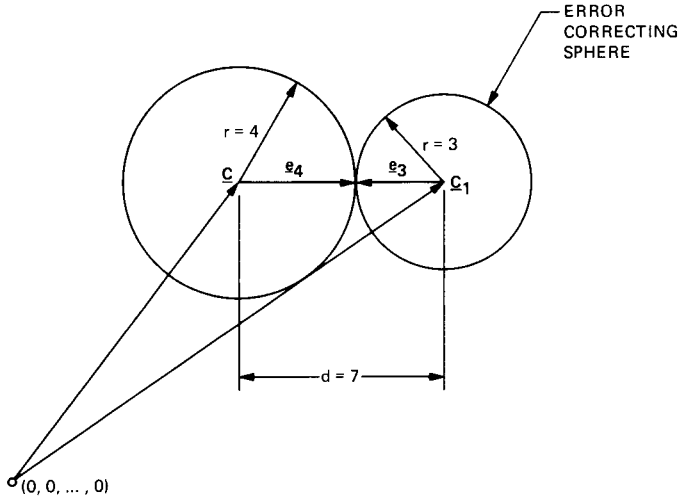


Fig. 1. A geometric view of the proof of Theorem 1.

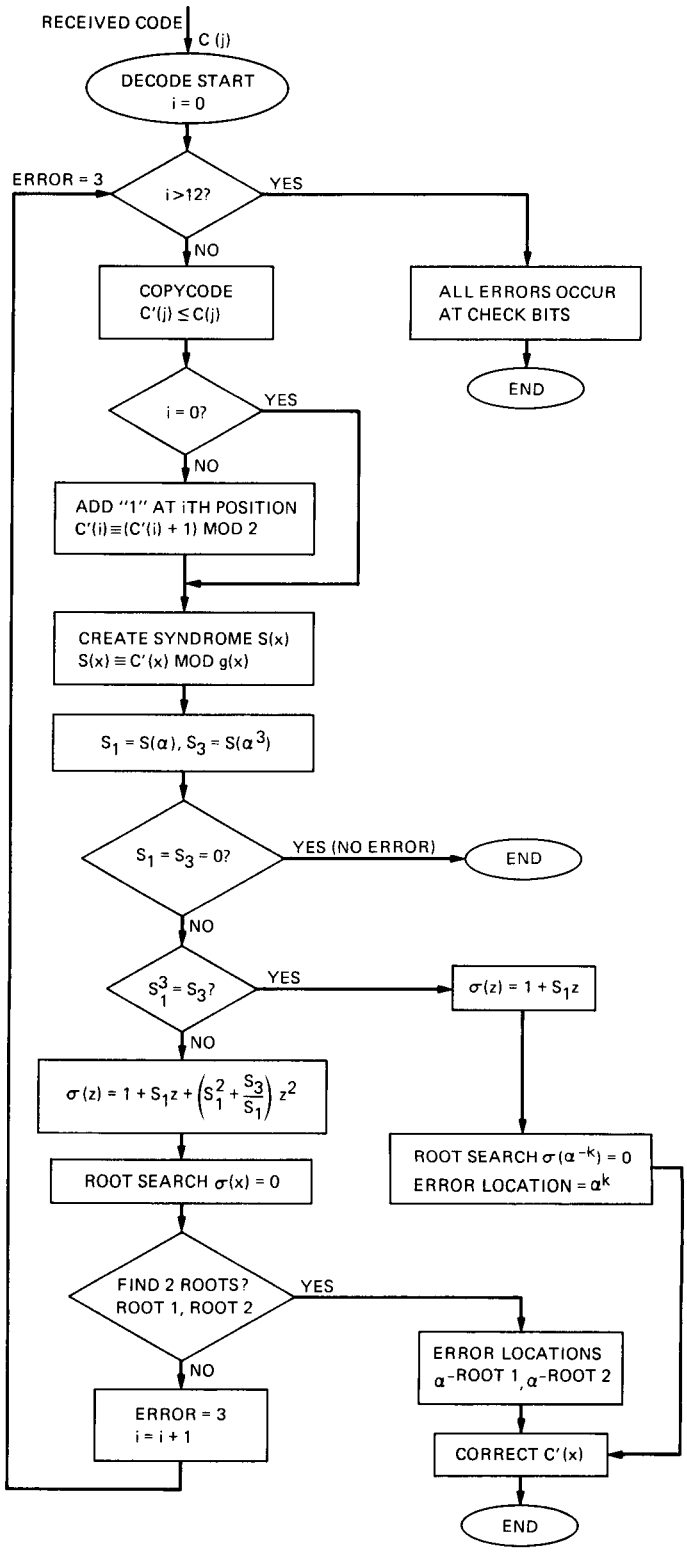


Fig. 2. Flowchart of the decoding algorithm.

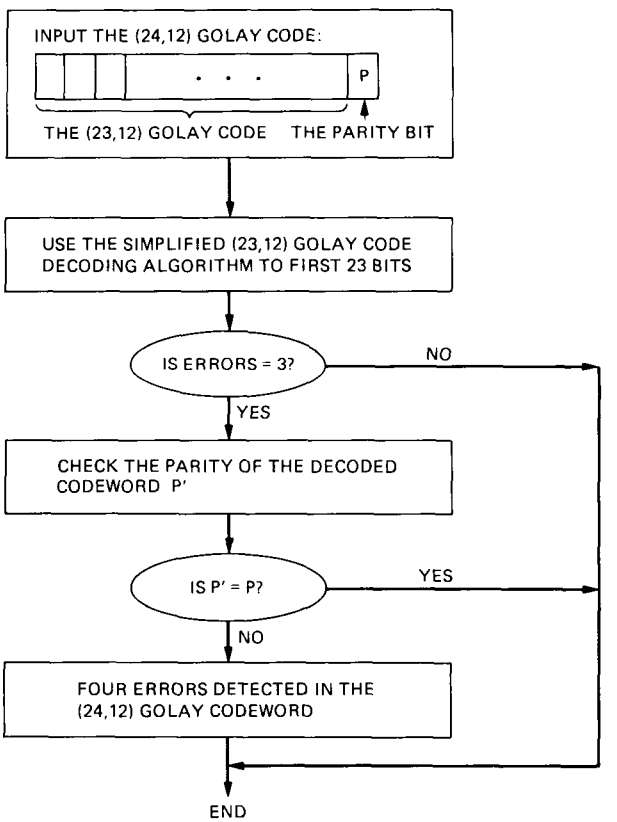


Fig. 3. The decoding flowchart of the (24, 12) Golay code.

Test Aspects of the JPL Viterbi Decoder

M. A. Breuer[1]
University of Southern California, Department of Electrical Engineering

This article deals with the generation of test vectors and design-for-test aspects of the JPL VLSI Viterbi decoder chip. Each processor IC contains over 20,000 gates. To achieve a high degree of testability, a scan architecture is employed. The logic has been partitioned so that very few test vectors are required to test the entire chip. In addition, since several blocks of logic are replicated numerous times on this chip, test vectors need only be generated for each block, rather than for the entire circuit. These unique blocks of logic have been identified and test sets generated for them. The approach employed for testing was to use pseudo-exhaustive test vectors whenever feasible. That is, each cone of logic is tested exhaustively. Using this approach, no detailed logic design or fault model is required. All faults which modify the function of a block of combinational logic are detected, such as all irredundant single and multiple stuck-at faults.

I. Introduction

The Jet Propulsion Laboratory (JPL) is currently designing a new Long Constraint Length VLSI Viterbi Decoder to be used on many future NASA missions [1]. This decoder consists of 8,192 Viterbi butterfly processors. A Viterbi decoder processor IC contains 16 Viterbi butterfly processors, resulting in over 20,000 gates per chip, with each individual butterfly processor having a complexity of about 1,800 gates. To enhance testability, a scan architecture [2] has been used. In this article we first discuss how the processor can be subdivided into three major blocks. Then the test architecture of each block is discussed along with the resulting test vectors required to test each block. Modifications to the logic which will simplify testing are also mentioned.

[1]The author is a consultant to JPL's Communications Systems Research Section.

II. Architecture

Figure 1 shows the hierarchical design schema of the Viterbi decoder chip. Entities in ovals represent macros. Entities in rectangles represent units of logic to be tested, such as gates, flip flops, multiplexers, or full adders. A number in brackets, such as $[n]$, indicates that there are n such entities. For example, a VC (Viterbi chip) macro consists of one 16-BFLYS macro and two MI macros. Table 1 indicates the gate-flip/flop (F/F) complexity of the main logic blocks in this chip. Blocks A–H are identified in Fig. 1. Assuming a flip flop consists of about 10 gate equivalences, this chip consists of approximately 20,000 gates.

The test generation for the Viterbi chip is based upon the analysis of three major blocks and related logic, namely the Metric Computer, the Memory Interface, and the Add-Compare-Select units. Each will be discussed in a separate section.

A *cloud* of logic is defined to be a combinational logic circuit all of whose outputs are either inputs to flip flops or are primary outputs, and all of whose inputs are either primary inputs or outputs of flip flops.

Note that a cloud of logic can be tested independently of any other combinational logic. Also, if a cloud of logic is replicated, then the tests for one cloud can be used to test all the other replicated clouds.

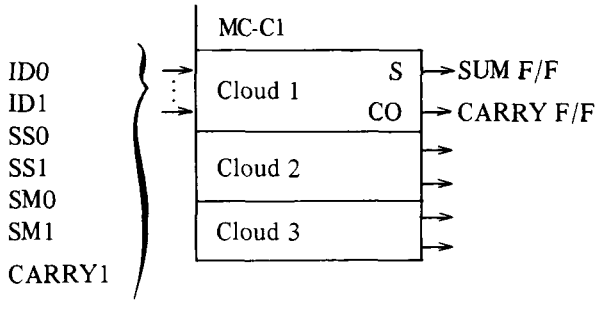
A *cone* of logic is defined to be a single-output combinational logic block whose output is either a primary output or an input to a flip flop, and whose inputs are either primary inputs or outputs of flip flops; every gate in the circuit which has a path through combinational logic to the output is in the cone.

A block of logic is said to be tested *pseudo-exhaustively* if an exhaustive test set is applied to each cone of the block.

III. Metric Computer

The architecture of the Metric Computer is shown in Figs. 2 and 3. Because of the feedback introduced by the carry flip flops, pipeline testing cannot be used. All flip flops are part of a scan chain. The combinational logic can be partitioned into four major blocks, namely MC-C1, MC-C2, MC-C3, and MC-C4 (see Fig. 3). The last three consist of only a full adder, and hence can be tested exhaustively with 8 test vectors. MC-C2 and MC-C3 have scan flip flops as drivers and receivers. MC-C4 has one primary input; the other I/O are scan flip flops.

MC-C1 has an architecture which can be decomposed into 3 clouds, as shown below.



MC-C1 has 7 X 3 = 21 inputs. To test MC-C1 exhaustively would require 2^{21} test vectors. However, each cloud has 7 inputs and can be tested exhaustively by $2^7 = 128$ test vectors. Due to the nature of the design, a pseudo-exhaustive test of just 8 test vectors exists. The test-vector set for the cloud shown in Fig. 4 is given in Table 2. The tests have been ordered so that C0 equals the next value of C, but this is not necessary. Note that when SM0 = 1, G1 is tested exhaustively; for SM1 = 1, G2 is tested exhaustively. Due to the fact that C0 implements a parity function, a sensitized path exists from G1 and G2 to a scan output. Thus, this test is a pseudo-exhaustive test for this cloud.

In summary, the Metric Computer can be tested with just 8 test vectors. The test is carried out as follows. A test vector is loaded into the scan flip flops. Simultaneously a test vector is loaded into the BFLY-ID shift registers. These two test vectors must be synchronized and aligned so that at time t, both scan chains are loaded. Then a normal clock is issued and all scan flip flops are loaded via their D input. The scan chain is then scanned out and the data checked. There are many ways for chaining flip flops to form a scan chain. The scan flip flops in the 16 Metric Computers can be put into one scan chain and then all Metric Computers can be tested as a unit by 8 test vectors. One Metric Computer has 6 flip flops in the BFLY-ID and 14 internal scan flip flops. The scan chain has 16 X 14 = 224 flip flops. Testing of the Metric Computers would take 8 + (224 X 8) = 1,800 clock cycles. The 8 comes from the 8 parallel-load clock cycles.

Figure 5 shows one possible scan path for this circuit.

Figure 6 indicates the BFLY-ID architecture. This circuit consists of one 6-bit shift register (SR) per Metric Computer. The 16 registers are connected together to form one long shift register. Only D flip flops are used; they are not scan flip flops and thus form what we refer to as a pseudo-scan chain.

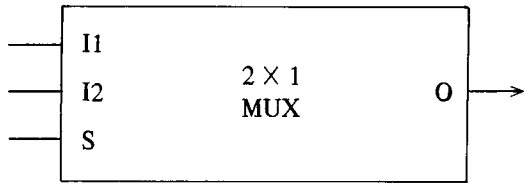
IV. Memory Interface Unit

There are two Memory Interface (MI) units. Each consists of a 16-bit parallel load shift register, as shown in Fig. 7(a). This unit both shifts and parallel loads as part of its normal operation, hence it has a unique $\overline{T}/R$ line, labeled LOAD. The register is made up of scan flip flops; the D inputs are used for parallel load; the scan-in for shifting data. This makes a double scan chain unnecessary. The four MIs share a common reset, clock, and load line. The parallel-in lines are driven by SELECT 0 ⟨31..16⟩; SELECT 0 ⟨15..0⟩; SELECT 1 ⟨31..16⟩; and SELECT 1 ⟨15..0⟩. The first SIN line to the unit should be tied to VDD or VSS. The RESET can be tested by loading in a vector consisting of all ones, resetting the flip flops, and scanning out the data and checking for all zeros.

The logic which drives each line is shown in Fig. 7(b) and consists of a scan flip flop and a MUX. There are 32 of these units. The architecture for the MI units and the logic which drives these units is shown in Fig. 7(c). The scan chain for the 12P flip flops is not identical to that shown in this figure. The

MUXs and MI units are tested by shifting a test vector into the register consisting of the 12P flip flops in the Compare-Select logic (CSL), passing it through the MUXs into the MI units, and shifting the data out of the MI units.

A 2 X 1 MUX is shown below.



A test for this device is shown below. S = 0 selects input I1; S = 1 selects input I2.

S	I1	I2	
0	0	1	Select I1 and pass a 0
0	1	0	Select I1 and pass a 1
1	0	1	Select I2 and pass a 0
1	1	0	Select I2 and pass a 1

To test the parallel load of a flip flop a 0 and a 1 are loaded. If the layout places lines close together in forming a register and there are possibilities of shorts, then an MI register can be loaded with the vectors 0101. . .01 and 1010. . .10. To test a shift register it is customary to pass a 0 and a 1. A pattern of the form 01100. . . is useful since it tests for the transitions 0 to 1 and 1 to 0, and the ability to hold a 0 and hold a 1.

The test vectors for this design are shown in Table 3. T1 loads zeros into the MI registers via the I1 input to all MUXs; T2 loads ones into the MI registers via the I1 input to all MUXs; T3 loads zeros via the I2 (FORCE) input to all MUXs; and T4 loads ones via the I2 (FORCE) input to all MUXs.

To load the MI registers with a more complex test pattern requires more test vectors. However, the test as proposed appears to be sufficient because it indirectly checks for hold and transition register operations; it does not test for shorts between adjacent register cells.

Since the 12P flip flops in the CSL do not form a scan chain, the bits in the test vectors must be distributed to the correct flip flops in the actual scan chain.

The testing of the MI units and associated logic consists of first scanning a test vector into the 12P flip flops of the 32 CSL units, next activating LOAD, FORCE, and FORCECTRL, and then shifting out the results from MI. Note that the 12P flip flops feed other logic and hence, later new data must be loaded to test this other logic. Overlaying these two test vector sets may be possible.

V. Add Compare Select (ACS)

Part of the logic of an ACS unit is shown in Fig. 8. The logic is driven primarily from flip flops 11P and 7P in the BFLY unit, and 13P and 14P in the METCOMP. The basic architectural structure is shown in Fig. 9. The logic in C2-ACS can be partitioned into clouds; one such cloud is shown in Fig. 10 along with the pseudo-exhaustive tests for this unit.

The testing of the MUXs 22P and 12P is straightforward, since their outputs drive scan flip flops and their inputs are either driven by primary inputs (CLOCK, WORD SYNC) or by scan flip flops.

Note that the clock input to flip flop 11P is from a MUX. During normal operation this clock is driven by the Q output of flip flop 8P. During scan mode this line is driven by CLOCK. Since the flip flops are edge triggered, a special test for this logic is necessary. One test vector is shown below.

					action
*A**	*B**	8PQ	11PQ	10P	11PQ
1	0	0	0	1	0 → 1

The scan chain is set up so that the conditions above are met. Then a normal-mode clock is issued. 8PQ will be set creating a 0 to 1 transition on the output of MUX 22P and setting flip flop 11PQ. A scan operation is then used to check the state of this flip flop. In a similar way a 0 can be loaded. No transition on the gated clock line can be produced. These conditions are summarized below.

					action	
*A**	*B**	8PQ	11PQ	10P	11PQ	8PQ
1	0	0	0	1	0 → 1	0 → 1
0	1	0	1	1	1 → 0	0 → 1
1	1	1	0	0	0 → 0	1 → 0
0	0	1	1	0	1 → 1	1 → 0

Note that these tests can be executed in the same way that other scan tests are executed, hence they are not really special.

A gate-level design of logic block C1-ACS is shown in Fig. 11(a). Also shown is a functional test set consisting of 24 vectors. The first block of vectors tests MUX 7P and establishes a sensitized path through MUX 18P, NAND gate 4P, and finally through MUX 13P. The next set of 4 vectors tests MUX 20P. The next set of 8 vectors tests the MUXs feeding NAND gate

3P. The final set of vectors tests 4P and 3P. Testing the final level of MUXs is done in a way such that all other MUXs are tested at the same time. There is some redundancy in this test set.

This circuit was processed using the USC Test Generation System (TGS). The results are shown in the Appendix. Figure A-1 shows the circuit description, which is an input to the program. Figure A-2 shows the functional test set. Figure A-3 shows the test vectors generated automatically using the PODEM algorithm. Only 16 test vectors are required to get 100 percent coverage of all single stuck-at faults. Figure A-4 shows the fault simulation results using the functional test vector set. This set also produced 100 percent fault coverage. However, 5 vectors can be deleted, reducing the test set to 19 vectors.

The discussion so far is incomplete since the ACS is not a fully scannable circuit, i.e., it contains an embedded shift register. Hence, when testing logic block C2-AC5, the results from A^* and B^* can be latched into the input to shift registers 1P and 9P. Then they can be shifted through these registers. The result from either A^* or B^*, but not both, can then be gated through MUXs 20P, 18P, and 13P into a scan flip flop SINK (see Fig. 8). This gating requires FORCE = 0 or 1, FORCE-CTRL = 1, RENORM TRIGGER = WORD SYNC = 0, K EQ 15 = 0, and ARITH CLOCK = $0 \rightarrow 1$.

Another problem exists because of these embedded shift registers. A test vector for logic block C1-ACS requires that certain values be applied to lines AP and BP. But these are outputs of the 16-bit shift registers. Hence, these values must occur at A^* and B^* 16 time periods earlier. Thus, the flip flops 11P, 7P, 13P, 14P, and the carry flip flops f20P and f30P must be set to proper values to produce the desired values of A^* and B^*. A test for C1-ACS consists of loading the scan chain with a test vector to produce the desired values of A^* and B^*, issuing 16 more clocks to drive the data through the 16-bit shift registers, and then issuing one more normal clock to load the result of the test into SINK. Then the scan chain can be read out.

To alleviate these problems, the 16-bit shift register consisting of 16 non-scan D flip flops can be modified to have the design shown in Fig. 12. Here the first and last flip flops of the shift register consist of scannable D flip flops. Now A^* and B^* are observable as part of a normal scan chain, and AP and BP are controllable as part of a normal scan chain. To test the shift register, a 0 can be scanned into 17P, and 15 normal clocks issued. The result in 20P can then be scanned out. This can then be repeated for 17P set to 1. This test is a slight modification of the normal scan test schema, in which after a scan operation, only one normal mode clock is issued.

VI. Conclusion

In this article it has been shown how the Viterbi decoder chip can be partitioned into very simple blocks of logic and test vectors generated for each such block. Most logic blocks are tested exhaustively, hence any permanent irredundant fault should be detected. It has also been indicated where normal scan design rule violations appear, and ways for overcoming these situations have been suggested.

It has not yet been determined how many scan chains should be used, which flip flops should go into which scan chains, and what the order of the flip flops in each scan chain should be. A flat design needs to be obtained so that test vectors for the entire scan chain can be determined. This will require the development of several programs, such as a test-set editor and a procedure to identify identical blocks of logic in the circuit, where in most cases each such block is a cloud. Testing parts of this circuit as a pipeline circuit is a possibility which would permit replacement of many of the scan flip flops by normal D flip flops.

Acknowledgment

The author would like to acknowledge Mr. Kuen-Jong Lee, whose efforts produced the results shown in the Appendix.

References

[1] J. Statman, G. Zimmerman, F. Pollara, and O. Collins, "A Long Constraint Length VLSI Viterbi Decoder for the DSN," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 134–142, November 15, 1988.

[2] I. S. Hsu, "On Testing VLSI Chips for the Big Viterbi Decoder," *TDA Progress Report 42-96*, this issue.

Table 1. Logic complexity

Block	Hardware component count (inverters not counted) No. of units	Gates	MUX	FA	F/Fs	Totals Gates	F/Fs
A	144	0	0	1(5)	2	720	288
B	80	0	0	1(5)	2	400	160
C	16	0	0	0	6	0	96
D	64	0	0	0	16	0	1024
E	32	4	6(18)	0	3	704	96
F	16	2	1	0	4	48	64
G	2	0	0	0	16	0	32
H	16	30	0	0	1	480	16
						2352	1776

FA (full adder) ≡ 5 gates
MUX (multiplexer) ≡ 3 gates
EOR (exclusive or) ≡ 4 gates

Table 2. Test for logic of Figure 4

Test Vector No.	I* D 0	S* S 0	I* D 1	S* S 1	G 1	G 2	S* M 0	S* M 1	FA Inputs A = G 7	B = G 8	C* = C +	FA Outputs S	C 0
1	0	1	0	1	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	1	1	1	0	1	0	1	0
3	0	0	1	0	1	0	1	1	1	0	0	1	0
4	0	0	0	0	1	1	1	1	1	1	0	0	1
5	0	0	0	0	1	1	1	1	1	1	1	1	1
6	1	1	1	1	1	1	1	0	1	0	1	0	1
7	1	1	1	1	1	1	0	1	0	1	1	0	1
8	0	1	0	1	0	0	1	1	0	0	1	1	0

*Inputs

Table 3. Test for MI units

	Tests 1	2	3	4
12P	0	1	0	1
FORCE	1	0	1	0
FORCE CNTL	0	0	1	1

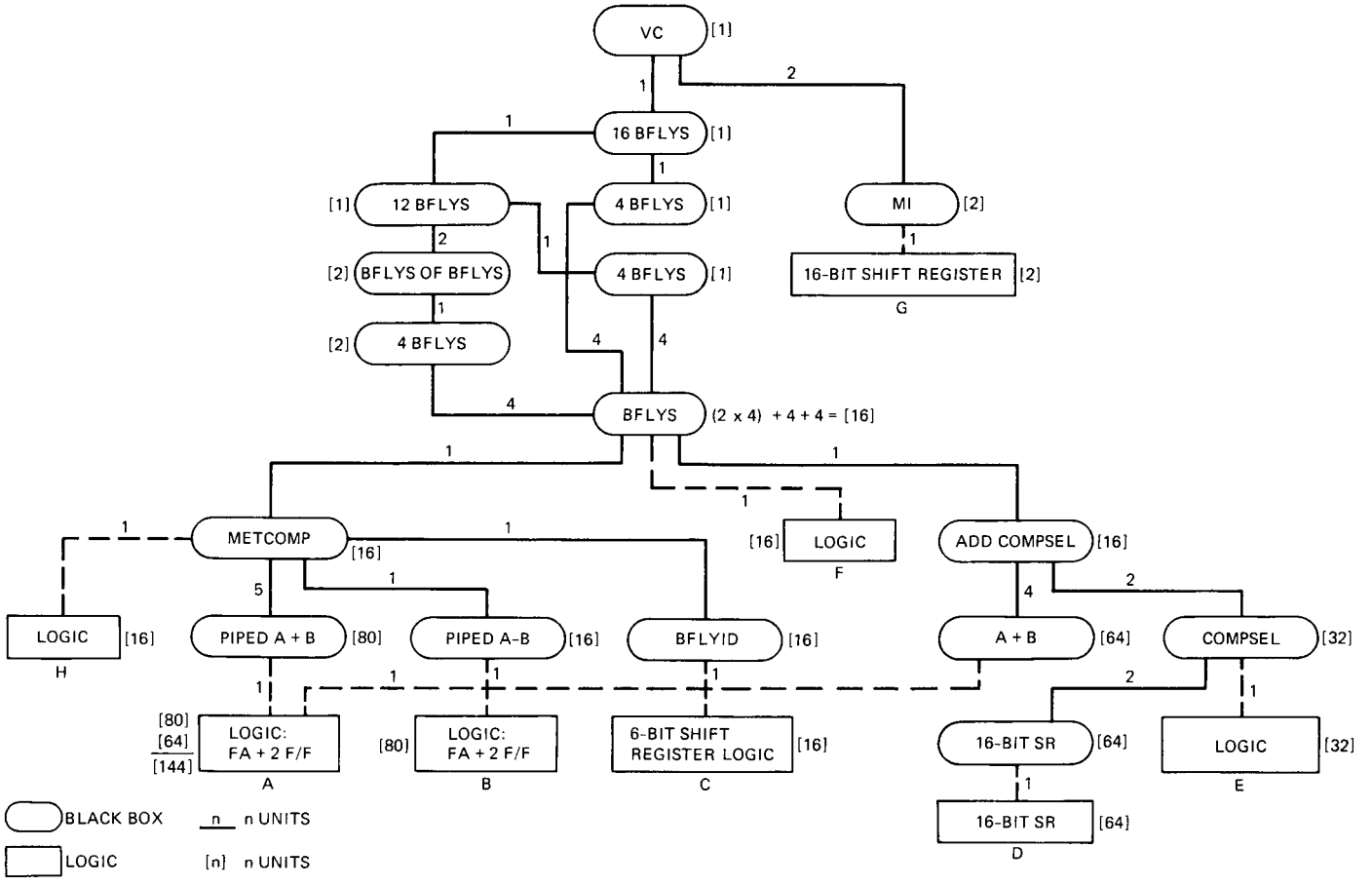


Fig. 1. Hierarchical design of Viterbi Decoder chip.

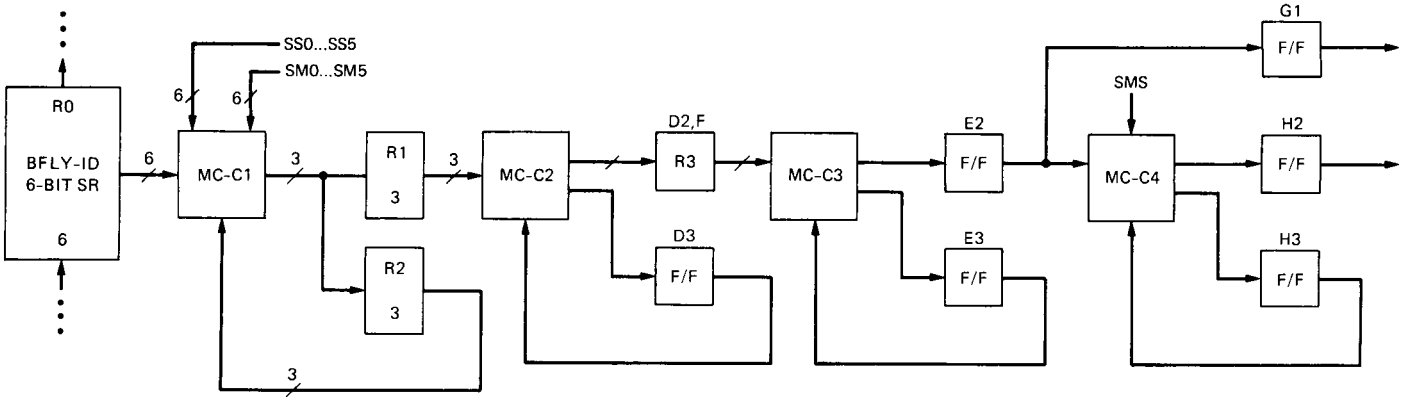


Fig. 2. General RT structure of Metric Computer.

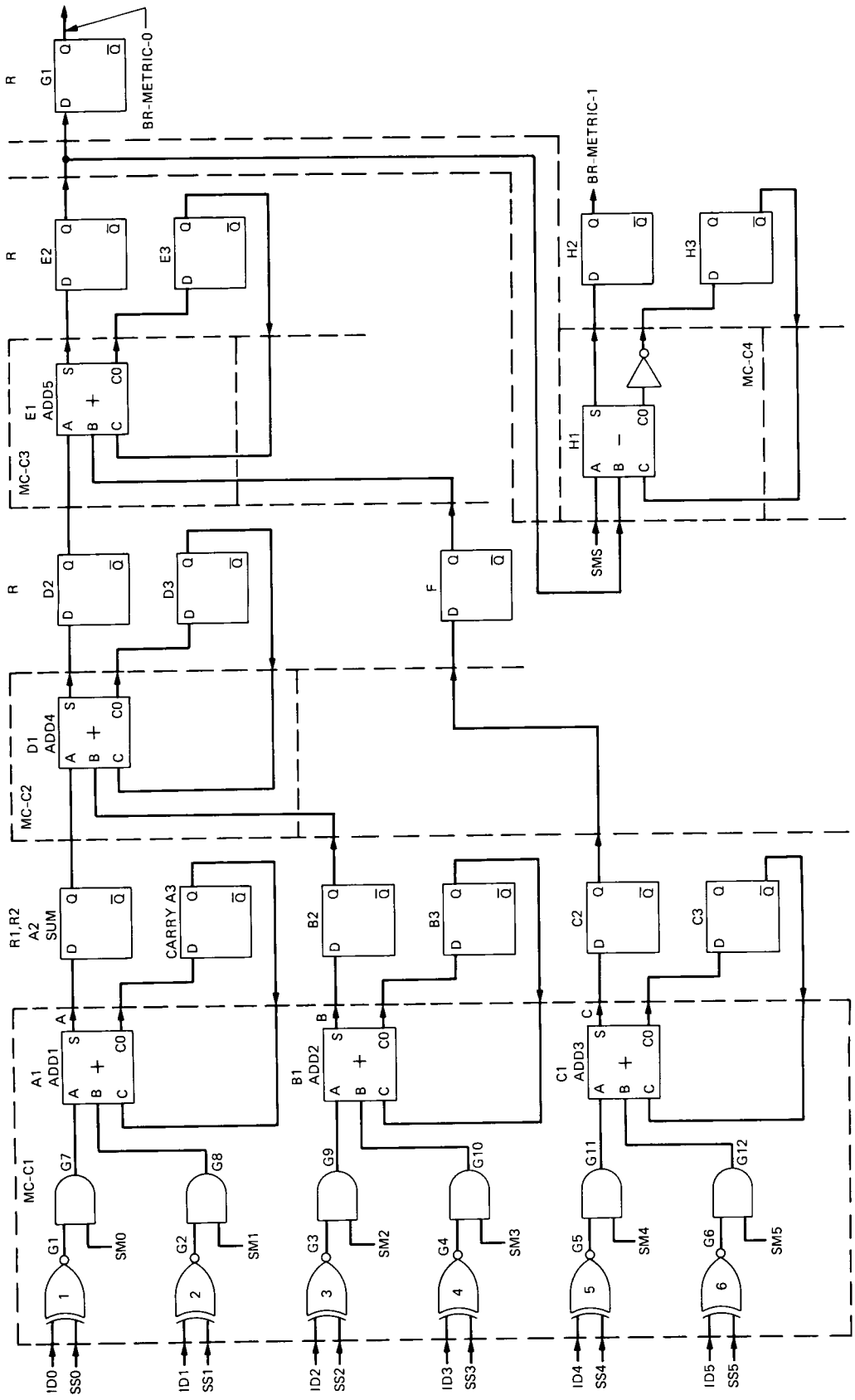


Fig. 3. Logic structure of Metric Computer.

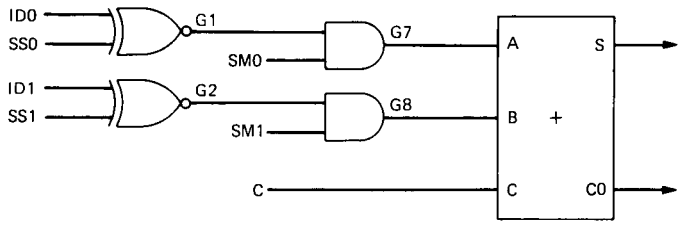


Fig. 4. One cloud in the Metric Computer.

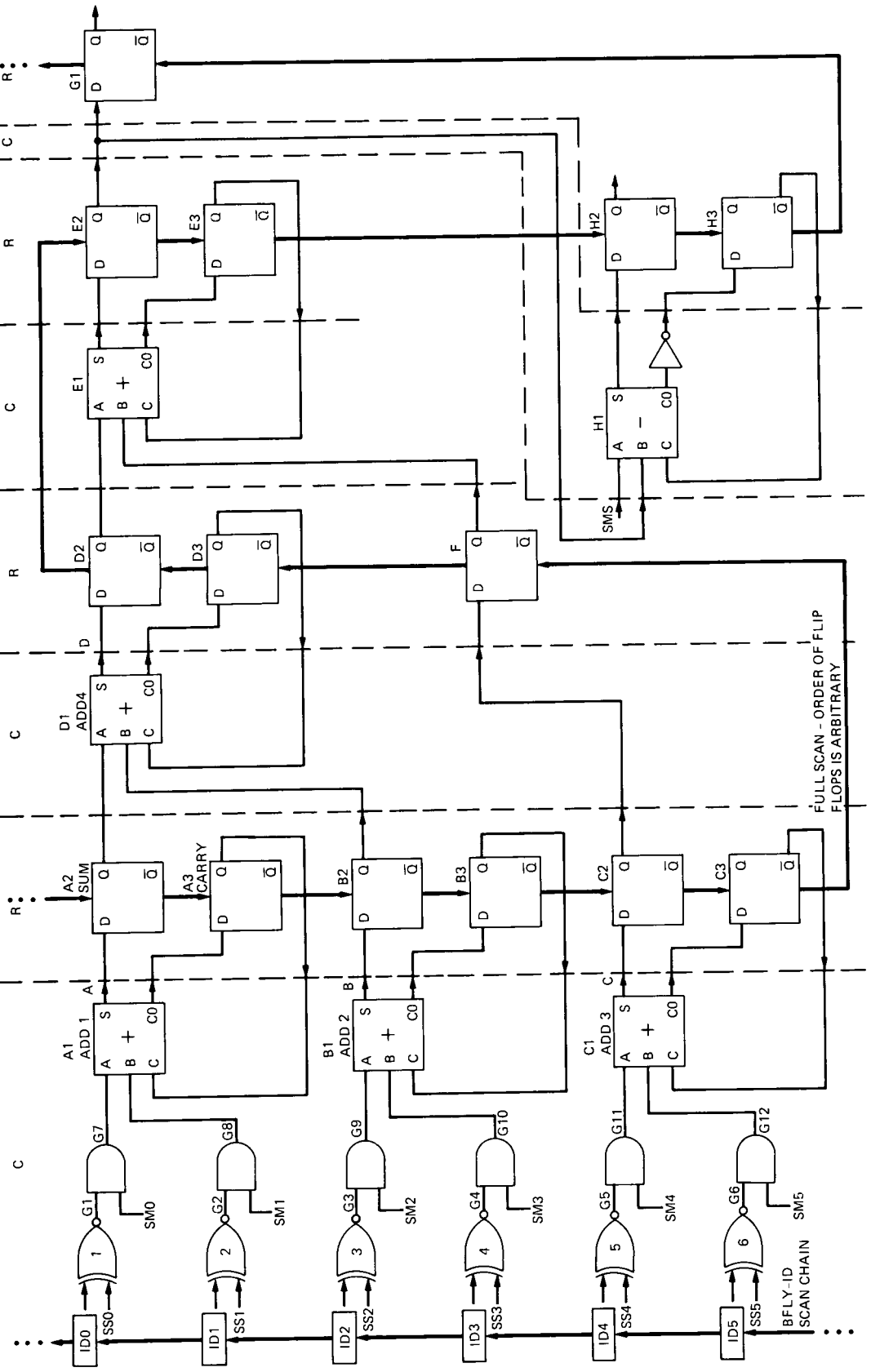


Fig. 5. Scan path in the Metric Computer.

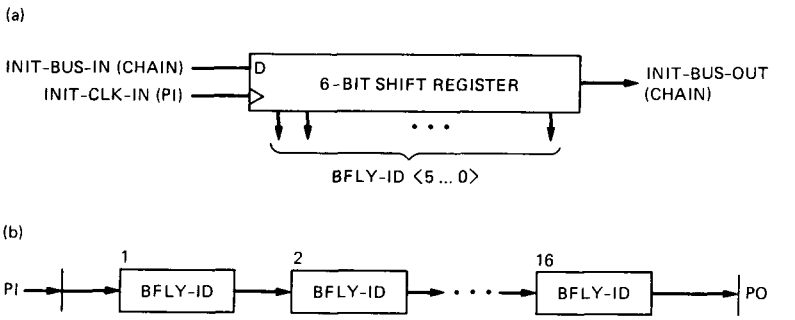


Fig. 6. BFLY-ID scan-chain architecture in the Metric Computer: (a) D flip flops forming a 6-bit shift register; and (b) 32 registers connected together to form one long shift register.

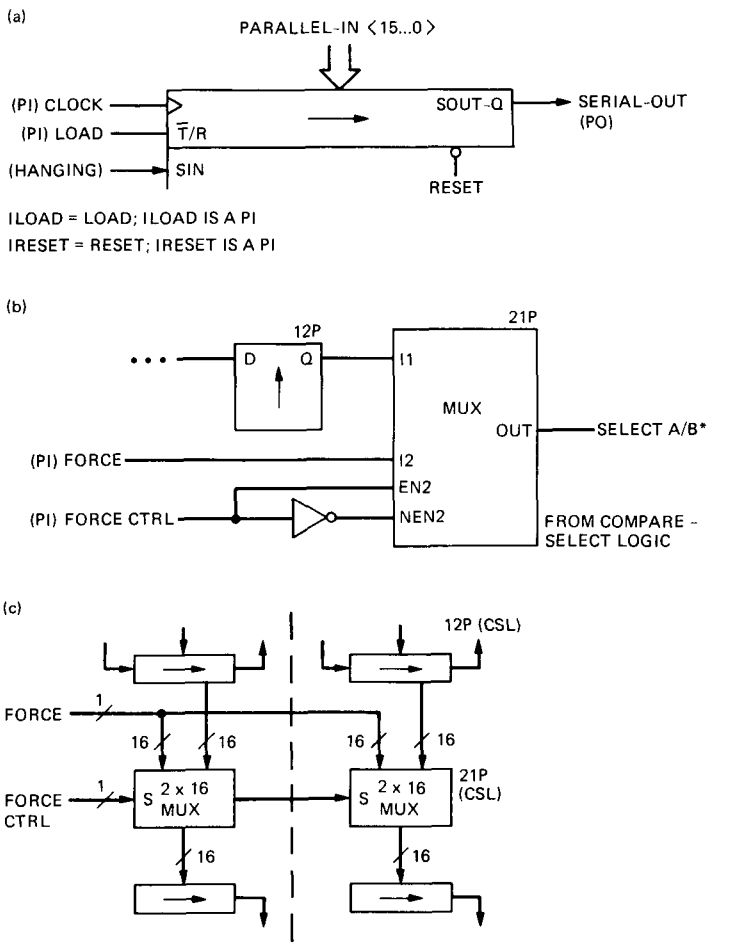


Fig. 7. Memory Interface: (a) one memory-interface unit; (b) logic driving a memory interface unit; and (c) architecture for 4 units.

FOLDOUT FRAME

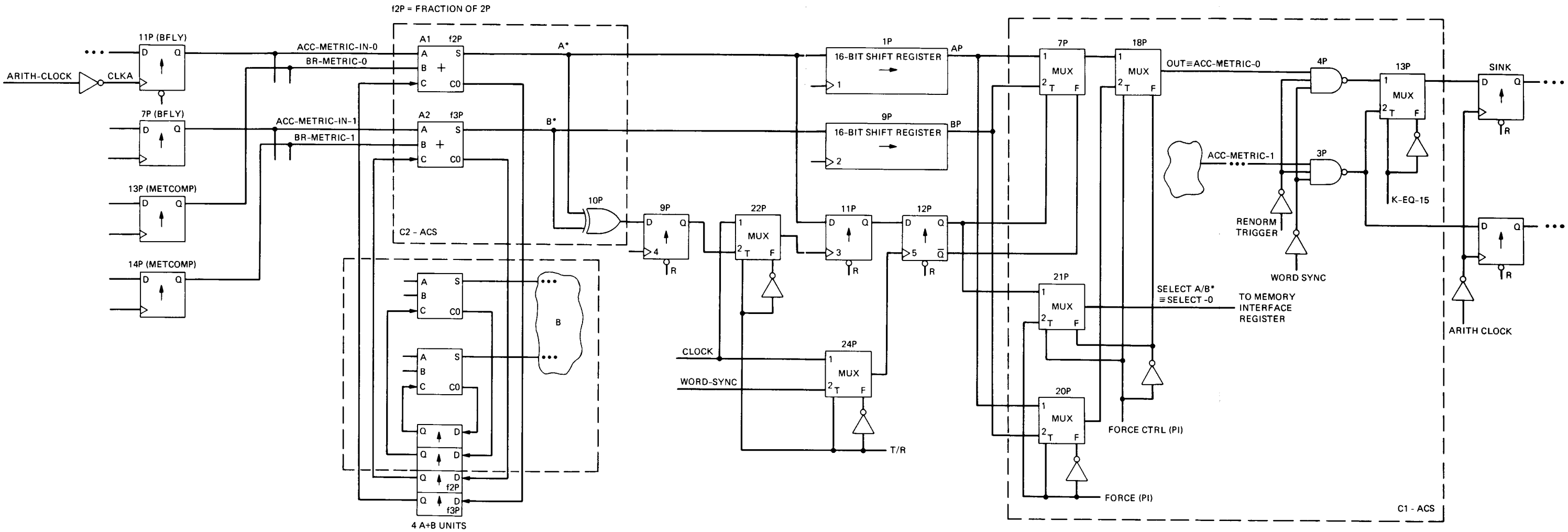


Fig. 8. Add-Compare-Select Unit block diagram.

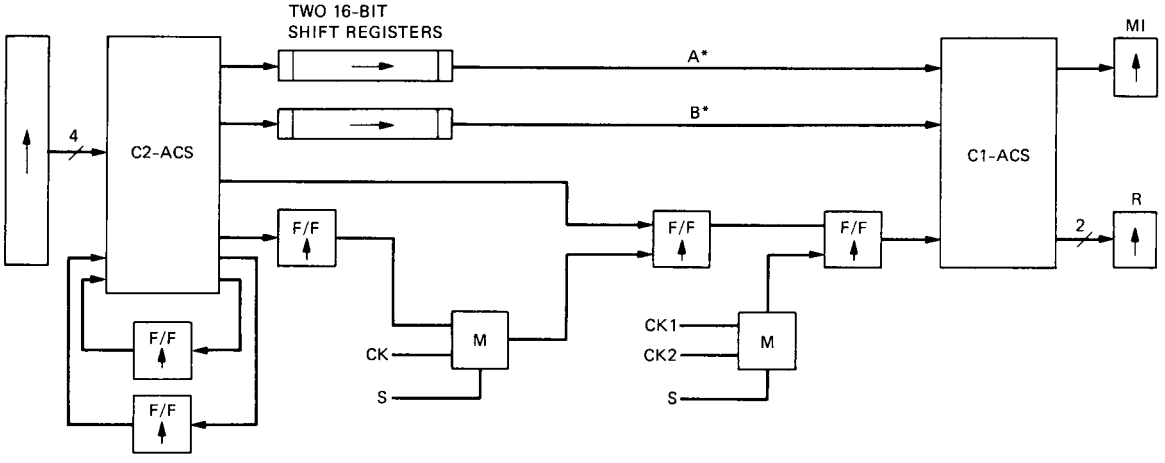
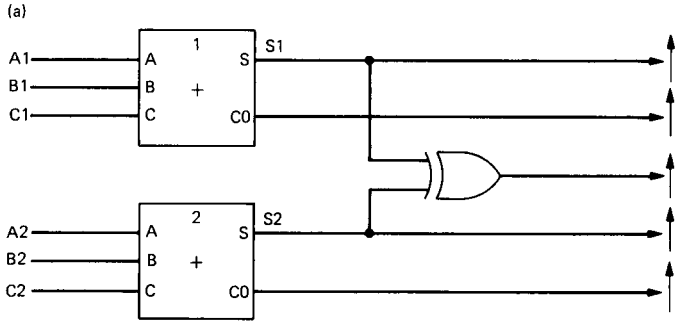


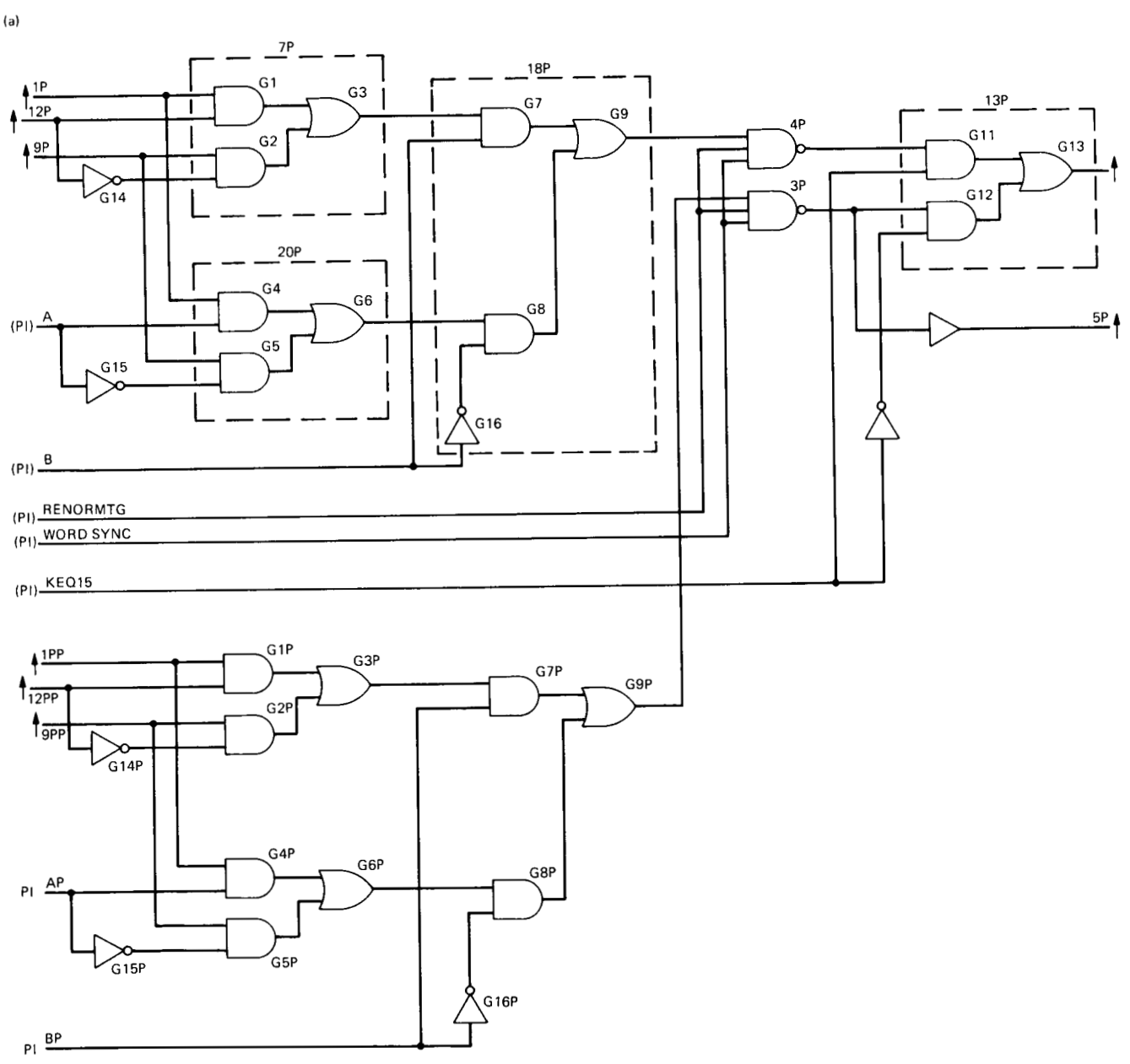
Fig. 9. Basic architectural structure of an Add-Compare-Select unit.



(b)

	A1	B1	C1	A2	B2	C2	S1	S2
T1	0	0	0	1	1	1	0	1
T2	0	0	1	0	0	0	1	0
T3	0	1	0	0	0	1	1	1
T4	0	1	1	0	1	0	0	1
T5	1	0	0	0	1	1	1	0
T6	1	0	1	1	0	0	0	1
T7	1	1	0	1	0	1	0	0
T8	1	1	1	1	1	0	1	0

Fig. 10. Logic block C2–ACS: (a) logic of a cloud and (b) test vectors. Adders 1 and 2, and the EOR gate are tested exhaustively.



(b)

RENORMTG — WORD SYNC

	1 9 12 PPPAB	KEQ15	WORD	1 9 12 PPPAB
7P	1 0 0 X 1	1 1 1		
	0 1 0 X 1	1 1 1		
	1 0 1 X 1	1 1 1		
	0 1 1 X 1	1 1 1		
20P	1 0 X 0 0	1 1 1		
	0 1 X 0 0	1 1 1		
	1 0 X 1 0	1 1 1		
	0 1 X 1 0	1 1 1		
		0 1 1		1 0 0 X 1
		0 1 1		0 1 0 X 1
		0 1 1		1 0 1 X 1
	×	0 1 1	×	0 1 1 X 1
		0 1 1		1 0 X 0 0
		0 1 1		0 1 X 0 0
		0 1 1		1 0 X 1 0
		0 1 1		0 1 X 1 0
4P	1 X 1 X 1 1 1 1	"1"		
	0 X 1 X 1 1 1 1	"0"	×	
	1 X 1 X 1 1 1 0	"1"		
	1 X 1 X 1 1 0 1	"1"		
3P		0 1 1		1 X 1 X 1
	×	0 1 1		0 X 1 X 1
		0 1 0		1 X 1 X 1
		0 0 1		1 X 1 X 1

24 FUNCTIONAL TEST VECTORS

Fig. 11. (a) Logic block C1–ACS and (b) functional test vectors.

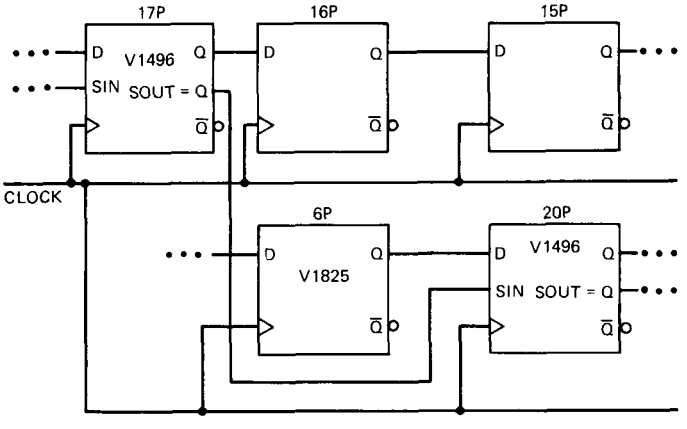


Fig. 12. Modified 16-bit shift register.

Appendix

Test Generation System Results

This Appendix contains the results of using the TGS on the combinational logic in the ACS unit. It consists of Figs. A-1 – A-4.

```
                          NO. OF    NO. OF
TYPE      NAME            FAN-OUT   FAN-IN
44
inpt      1p              2         0
inpt      9p              2         0
inpt      12p             2         0
inpt      a               2         0
inpt      b               2         0
inpt      keql5           2         0
inpt      renormtg        2         0
inpt      wordsync        2         0
inpt      1pp             2         0
inpt      9pp             2         0
inpt      12pp            2         0
inpt      ap              2         0
inpt      bp              2         0
                                              FAN-IN LIST
and       gl              1         2         1p          12p
inv       gl4             1         1         12p
and       g2              1         2         9p          gl4
or        g3              1         2         gl          g2

and       g4              1         2         1p          a
inv       gl5             1         1         a
and       g5              1         2         9p          gl5
or        g6              1         2         g4          g5

and       g7              1         2         g3          b
inv       gl6             1         1         b
and       g8              1         2         g6          gl6
or        g9              1         2         g7          g8

and       glp             1         2         1pp         12pp
inv       gl4p            1         1         12pp
and       g2p             1         2         9pp         gl4p
or        g3p             1         2         glp         g2p

and       g4p             1         2         1pp         ap
inv       gl5p            1         1         ap
and       g5p             1         2         9pp         gl5p
or        g6p             1         2         g4p         g5p

and       g7p             1         2         g3p         bp
inv       gl6p            1         1         bp
and       g8p             1         2         g6p         gl6p
or        g9p             1         2         g7p         g8p

nand      4p              1         3         g9          renormtg wordsync
nand      3p              2         3         g9p         renormtg wordsync

and       gll             1         2         4p          keql5
inv       gl7             1         1         keql5
and       gl2             1         2         3p          gl7
or        gl3             0         2         gll         gl2

buf       5p              0         1         3p
```

Fig. A-1. Circuit input description.

(a)

12345	678	1111 90123
100x1	111	xxxxx
010x1	111	xxxxx
101x1	111	xxxxx
011x1	111	xxxxx
10x00	111	xxxxx
01x00	111	xxxxx
10x10	111	xxxxx
01x10	111	xxxxx
xxxxx	011	100x1
xxxxx	011	010x1
xxxxx	011	101x1
xxxxx	011	011x1
xxxxx	011	10x00
xxxxx	011	01x00
xxxxx	011	10x10
xxxxx	011	01x10
lxlxl	111	xxxxx
0xlxl	111	xxxxx
lxlxl	110	xxxxx
lxlxl	101	xxxxx
xxxxx	011	lxlxl
xxxxx	011	0xlxl
xxxxx	010	lxlxl
xxxxx	001	lxlxl

(b)

1	1P
2	9P
3	12P
4	A
5	B
6	K EQ 15
7	RENORMTG
8	WORD SYNC
9	1PP
10	9PP
11	12PP
12	AP
13	BP

Fig. A-2. (a) Functional test vectors and (b) corresponding column headings.

```
Please enter circuit file name: cfunc


                MAIN MENU

            0. Exit
            1. Fault-collapsing
            2. Test-generation
            3. Fault-simulation
            4. Logic-simulation
            5. Integrated System

          Please enter your choice: 5

 Would you like to use the following default values?

    Exiting Condition : fault coverage = 100%
    In-order fault selection
    Test Generation Method : PODEM

   Please enter: [y/n] y

For the following file names, enter
 <RETURN> to use default file name as shown in parentheses,
    "/"   to suppress file generation, or
  enter the desired name.

Please enter file name for fault classes.
 (default name: cfunc.cls) :
Please enter file name for resulting test vectors.
 (default name: cfunc.tst) :
Please enter file name for fault list.
 (default name: cfunc.flt) :
Please enter file name for complete output result.
 (default name: cfunc.res) :
Please enter file name for execution time.
 (default name: cfunc.tim) :

If there is any "x" (don't care) in the test vector,
 what value should it be assigned?
    1. always assign "1"
    2. always assign "0"
    3. randomly assign "1" or "0"
 Enter your selection: 3
 Enter the probability of assigning "1": 0.6

 Please choose one option for fault collapsing:
   1  Equivalence merging only (for circuits with feedback).
   2  Equivalence as well as dominance merging.
 Enter option: 2

**** Fault Collapsing OK! ****

 Number of faults = 144

*** Now enter the main loop ... ***

Number of detected faults = 0
Current fault coverage is 0.00%

**************************************************
**************************************************
 First selection iteration..
------------------------------------------
Vector[1] is
11101 11111 111
Number of detected faults = 29
Current fault coverage is 20.14%
------------------------------------------
Vector[2] is
01111 11101 111
Number of detected faults = 58
Current fault coverage is 40.28%
------------------------------------------
Vector[3] is
10011 11100 110
Number of detected faults = 69
Current fault coverage is 47.92%
------------------------------------------
Vector[4] is
11011 11110 100
Number of detected faults = 83
Current fault coverage is 57.64%
------------------------------------------
Vector[5] is
10010 11100 101
Number of detected faults = 90
Current fault coverage is 62.50%
------------------------------------------
Vector[6] is
01110 11110 101
Number of detected faults = 97
Current fault coverage is 67.36%
------------------------------------------
Vector[7] is
10100 11110 110
Number of detected faults = 109
Current fault coverage is 75.69%
------------------------------------------
Vector[8] is
11000 11111 101
Number of detected faults = 113
Current fault coverage is 78.47%
------------------------------------------
Vector[9] is
10110 01010 011
Number of detected faults = 117
Current fault coverage is 81.25%
------------------------------------------
Vector[10] is
10001 11110 011
Number of detected faults = 123
Current fault coverage is 85.42%
------------------------------------------
Vector[11] is
10110 01111 011
Number of detected faults = 129
Current fault coverage is 89.58%
------------------------------------------
Vector[12] is
11101 01101 010
Number of detected faults = 132
Current fault coverage is 91.67%
------------------------------------------
Vector[13] is
11010 11111 000
Number of detected faults = 136
Current fault coverage is 94.44%
------------------------------------------
Vector[14] is
11001 10110 101
Number of detected faults = 139
Current fault coverage is 96.53%
------------------------------------------
Vector[15] is
01011 11011 100
Number of detected faults = 142
Current fault coverage is 98.61%
------------------------------------------
Vector[16] is
00011 01101 011
Number of detected faults = 144
Current fault coverage is 100.00%
**************************************************
**************************************************
 Total number of faults is 144.

 144 faults have been detected by 16 test vectors.
 The fault coverage is 100.0000 %.

**************************************************
```

Fig. A-3. Results of automatic test-vector generation.

```
Please enter circuit file name: cfunc


                    MAIN MENU

                0. Exit
                1. Fault-collapsing
                2. Test-generation
                3. Fault-simulation
                4. Logic-simulation
                5. Integrated System

Please enter your choice: 5

Would you like to use the following default values?

    Exiting Condition : fault coverage = 100%
    In-order fault selection
    Test Generation Method : PODEM

Please enter: [y/n] n

Which Test Generation method should be used?
    1. PODEM
    2. Random Test Generation
    3. Test Vectors in a file
Enter your selection: 3

Which exiting condition do you wish to use ?
    1. fault coverage
    2. number of test vectors
    3. CPU time (not available)
Enter your selection: 1

Please enter the percentage fault coverage desired: 100

                FUNCTIONAL TEST VECTORS

Please enter input file name for test vectors.
 <RETURN> --- use default name: cfunc.int
    Enter:
For the following file names, enter
 <RETURN> to use default file name as shown in parentheses,
    "/"   to suppress file generation, or
  enter the desired name.

Please enter file name for fault classes.
 (default name: cfunc.cls) : cfuncl.cls
Please enter file name for resulting test vectors.
 (default name: cfunc.tst) : cfuncl.tst
Please enter file name for fault list.
 (default name: cfunc.flt) : cfuncl.flt
Please enter file name for complete output result.
 (default name: cfunc.res) : cfuncl.res
Please enter file name for execution time.
 (default name: cfunc.tim) : cfuncl.tim

If there is any "x" (don't care) in the input vector,
what value should it be assigned?
    1. always assign "1"
    2. always assign "0"
    3. randomly assign "1" or "0"
Enter your selection: 3
Enter the probability of assigning "1": 0.6

Please choose one option for fault collapsing:
    1  Equivalence merging only (for circuits with feedback).
    2  Equivalence as well as dominance merging.
Enter option: 2

**** Fault Collapsing OK! ****

Number of faults = 144

*** Now enter the main loop ... ***

Number of detected faults = 0
Current fault coverage is 0.00%
-----------------------------------------------
Vector[1] is
10011 11101 111
Number of detected faults = 31
Current fault coverage is 21.53%
-----------------------------------------------
Vector[2] is
01011 11111 011
Number of detected faults = 62
Current fault coverage is 43.06%
-----------------------------------------------
Vector[3] is
10111 11111 001
Number of detected faults = 66
Current fault coverage is 45.83%
-----------------------------------------------
Vector[4] is
01111 11101 110
Number of detected faults = 78
Current fault coverage is 54.17%
-----------------------------------------------
Vector[5] is
10100 11100 000
Number of detected faults = 88
Current fault coverage is 61.11%
-----------------------------------------------
Vector[6] is
01000 11110 111
Number of detected faults = 100
Current fault coverage is 69.44%
-----------------------------------------------
Vector[7] is
10110 11101 011
Number of detected faults = 103
Current fault coverage is 71.53%
-----------------------------------------------
Vector[8] is
01110 11101 101
Number of detected faults = 110
Current fault coverage is 76.39%
-----------------------------------------------
Vector[9] is
01110 01110 011
Number of detected faults = 117
Current fault coverage is 81.25%
-----------------------------------------------
Vector[10] is
10110 01101 011
Number of detected faults = 118
Current fault coverage is 81.94%
-----------------------------------------------
Vector[11] is
10011 01110 111
Number of detected faults = 120
Current fault coverage is 83.33%
-----------------------------------------------
*Vector[12] is
 00011 01101 111
 Number of detected faults = 120
 Current fault coverage is 83.33%
-----------------------------------------------
 Vector[13] is
 10110 01110 000
 Number of detected faults = 122
 Current fault coverage is 84.72%
-----------------------------------------------
 Vector[14] is
 11111 01101 000
 Number of detected faults = 130
 Current fault coverage is 90.28%
-----------------------------------------------
 Vector[15] is
 10011 01110 010
 Number of detected faults = 133
 Current fault coverage is 92.36%
-----------------------------------------------
*Vector[16] is
 10110 01101 110
 Number of detected faults = 133
 Current fault coverage is 92.36%
-----------------------------------------------
 Vector[17] is
 10111 11101 010
 Number of detected faults = 138
 Current fault coverage is 95.83%
-----------------------------------------------
*Vector[18] is
 01111 11111 000
 Number of detected faults = 138
 Current fault coverage is 95.83%
-----------------------------------------------
 Vector[19] is
 11101 11010 100
 Number of detected faults = 140
 Current fault coverage is 97.22%
-----------------------------------------------
 Vector[20] is
 11111 10101 010
 Number of detected faults = 142
 Current fault coverage is 98.61%
-----------------------------------------------
*Vector[21] is
 01101 01110 111
 Number of detected faults = 142
 Current fault coverage is 98.61%
-----------------------------------------------
*Vector[22] is
 11101 01101 101
 Number of detected faults = 142
 Current fault coverage is 98.61%
-----------------------------------------------
 Vector[23] is
 10000 01010 111
 Number of detected faults = 143
 Current fault coverage is 99.31%
-----------------------------------------------
 Vector[24] is
 11100 00110 101
 Number of detected faults = 144
 Current fault coverage is 100.00%
 ************************************************
 ************************************************
  Total number of faults is 144.

  144 faults have been detected by 24 test vectors.
  The fault coverage is 100.0000 %.

 ************************************************
 *These vectors can be deleted.
```

Fig. A-4. Results of fault simulation for functional test vectors.

57-33
P- 13
193059

TDA Progress Report 42-96

October–December 1988

N89-19458

On Testing VLSI Chips for the Big Viterbi Decoder

I. S. Hsu

Communications Systems Research Section

A general technique that can be used in testing very large scale integrated (VLSI) chips for the Big Viterbi Decoder (BVD) system is described in this article. The test technique is divided into functional testing and fault-coverage testing. The purpose of functional testing is to verify that the design works functionally. Functional test vectors are converted from outputs of software simulations which simulate the BVD functionally. Fault-coverage testing is used to detect and, in some cases, to locate faulty components caused by bad fabrication. This type of testing is useful in screening out bad chips. Finally, 'design for testability,' which is included in the BVD VLSI chip design, is described in considerable detail in this article. Both the observability and controllability of a VLSI chip are greatly enhanced by including the design for testability feature.

I. Introduction

A concatenated system which uses a (255,223) Reed-Solomon outer code and a (7,1/2) Viterbi-decoded convolutional inner code has been recommended by the Consultative Committee for Space Data Systems (CCSDS) [1] as a standard channel-coding scheme for the future DSN. This concatenated scheme will provide an additional 2 dB in coding gain at a bit error rate (BER) of 10^{-5} over a Viterbi-decoded-only channel [2]. However, there is a need for even greater coding gain in future missions such as Galileo. A recent JPL Research and Technology Objectives and Plans (RTOP) activity showed that an additional 2 dB coding gain over the concatenated coding channel recommended by CCSDS can be achieved by concatenating a (1023,959) Reed-Solomon code with a (15,1/6) Viterbi-decoded convolutional code [3].

A VLSI-based BVD for convolutional codes is described in [4]. It will be able to decode convolutional codes with constraint length K from 1 to 15 and code rate varying from 1/2 to 1/6. The difficulty in building the BVD is the large number of states in the Viterbi decoding algorithm [5], which grow exponentially with K. For example, there are 2^{14} states in a (15,1/6) Viterbi decoder. These 2^{14} states can be configured as 2^{13} butterflies, each butterfly consisting of two states. Each state performs add, compare, and select operations [4] with an operation speed of 1 Mbit/sec. Implementing such a large number of butterflies in silicon with current technology is an extremely difficult task.

Bit-serial arithmetic is used in the BVD [4] to simplify the complexity caused by the large number of states. It is shown in [3] that the 2^{13} butterflies in the (15,1/6) Viterbi decoder can be implemented with 512 identical VLSI chips using 1.5-μm complementary-metal-oxide-semiconductor (CMOS) technology. Each chip contains 16 butterflies. It is estimated that each chip will contain about 20,000 gates where a gate corresponds to a standard two-input CMOS NotAnd (NAND) gate which contains four transistors. Because of the large

number of gates, the implementation of this chip must be carefully planned and should include a comprehensive testing strategy.

Testing of VLSI chips can be divided into functional testing and fault-coverage testing. Functional testing verifies that the VLSI design functions as expected. The fault-coverage test is used to detect and, in some cases, to locate faulty components on a fabricated VLSI chip. Diagnostic procedures are carried out to determine if the faulty components are caused by bad fabrication or design errors. The detected errors can be corrected in a subsequent fabrication run if a design problem is found.

This article describes a testing technique that will be used in developing the BVD VLSI chip. A tutorial on fault simulation and design for testability is also provided. In Section II, the planned functional testing procedure for the (15,1/6) VLSI-based Viterbi decoder is described. Section III describes techniques that can be used for fault-coverage testing. Several techniques to increase design for testability of a VLSI chip are illustrated in Section IV in considerable detail. The technique used to enhance design for testability of the BVD VLSI chips is described in Section V. Finally, some concluding remarks are made in Section VI.

II. Functional Testing of VLSI Chips

The Big Viterbi Decoder system utilizes bit-serial arithmetic to reduce the complexity as well as increase operational speed of the VLSI chip [4]. In order to implement the 2^{13} butterflies in the BVD system with current 1.5-μm CMOS technology, 512 identical VLSI chips are required. Each VLSI chip contains 16 butterflies; each butterfly contains two states. Figure 1 shows the functional diagram of the BVD and Fig. 2 depicts a block diagram of a butterfly. Figure 3 shows a logic diagram of the metric computation unit in a butterfly.

A software simulator has been written to mimic the operation of the bit-serial BVD hardware [6]. The outputs of the software simulator are converted into functional test vectors for the BVD VLSI chips. The following example illustrates the procedure of generating the functional test vectors. In Fig. 4, which depicts a sample software simulator output, r_i (received messages) are represented in octal numbers. Thus, r_i equals 227 in octal and 10010111 in binary representation. Also in Fig. 4, "label" denotes the identification of a butterfly [6], p and q represent the branch metrics computed from the corresponding received messages r_i, x is the sum of magnitudes of the received symbols, m_{i0}, m_{j0} are the old accumulated metrics, and m_{i1}, m_{j1} are the new accumulated metrics of the two states in the butterfly. Based on the outputs of the software simulator, functional test vectors for the metric computation unit are generated. These functional test vectors are manually entered into the VAX computer using a program called "Logic," developed at JPL.[1] The output files generated by "Logic" are in "rsim"[2] format which is widely used to represent logic vectors in university-based VLSI CAD systems. Both the system hardware and VLSI designs of the BVD are performed with the Valid workstation [7]. A translator called "RSIM2VAL,"[3] also developed at JPL, is used to convert the output of "Logic" to a format that is acceptable to the Valid logic simulator.

A hierarchical approach [8] is used in designing BVD chips. For example, after full logic simulation of the branch metric computation unit (Fig. 3), functional test vectors are generated for testing combined blocks such as the branch metric and add/compare/select blocks depicted in Fig. 3. This process continues until functional testing of the entire chip is achieved.

After the VLSI chip layout passes logic simulations, circuit simulations, and design rule checking, it is ready to be shipped to the foundry for further checking procedures. For the BVD design, the foundry will perform fault simulation and some other check procedures to ensure that the VLSI chip design is error free. After the VLSI chip layout passes all the checking procedures by the foundry, it is ready for fabrication.

III. Techniques for Fault-Coverage Test of VLSI Chips

CMOS has been chosen as the fabrication technology for the VLSI chips in the BVD. Recently CMOS has been widely used because of its low power consumption, high density, high performance, and mature fabrication technology. The faults that most frequently occur in a CMOS circuit can be categorized into the following types:

(1) stuck-at-1 fault

(2) stuck-at-0 fault

(3) stuck-open fault

(4) stuck-short fault

---

[1] L. J. Deutsch, "Logic – Simulate and Test VLSI Circuits," Documentation of 1985 VLSI Tools (internal document), Communications Systems Research Section, Jet Propulsion Laboratory, Pasadena, California, 1985.

[2] L. J. Deutsch, "rsim – a Superset of the rnl Simulator with File Input," Documentation of 1985 VLSI Tools (internal document), Communications System Research Section, Jet Propulsion Laboratory, Pasadena, California, 1985.

[3] L. J. Deutsch, "rsim2val – a translator from rsim format to Valid format," Documentation of 1987 VLSI Tools (internal document), Communications Systems Research Section, Jet Propulsion Laboratory, Pasadena, California, 1987.

The stuck-at-1 fault refers to a specific node in the chip that is always stuck at logic level 1 regardless of the input conditions. The stuck-at-0 fault, on the contrary, means that the node is always at logic level 0. The stuck-open fault indicates that a driving transistor is always open in spite of the change of the input voltage applied to it. This fault may be caused by an oxide-layer imperfection created during fabrication or a faulty gate contact [9]. The stuck-short fault is the opposite effect. The transistor is always shorted regardless of the input voltage applied to the transistor. This fault is either due to pin holes created in the oxide layer during fabrication or the "punch-through" effect caused by excessive voltage applied to the drain terminal of the transistor [9]. Both the stuck-open and stuck-short faults are difficult to model and simulate because time-delay effects are introduced by these faults. A combinational circuit is changed into a sequential circuit by the time-delay effect. There is no good method developed so far to simulate sequential circuits for fault-coverage. Fortunately, most of the stuck-open and stuck-short faults are covered by the stuck-at-1 and stuck-at-0 faults [10]. Therefore, the stuck-open and stuck-short fault models are not mandatory. It has been reported that only 0.1 percent to 0.3 percent of the VLSI chips might have an undetected defect after passing test screens based on stuck-at fault only analysis [10].

Most of the existing VLSI fault-simulation programs deal with gate-level design. The fault simulation procedure can be divided into the following steps:

(1) Fault collapsing

(2) Test vector generation

(3) Fault simulation

After the logic schematic of a VLSI circuit is entered into the computer system, the fault simulator will perform fault collapsing. Given a combinational circuit, fault collapsing provides a number of fault classes. Each class consists of two fault sets: an equivalent set and a dominating set. Any test vector that can detect any one fault in an equivalent set will be able to detect all other faults in the same set. Any test vector that detects a fault in the equivalent set will also detect all the faults in the corresponding dominating set. However, it is not true that any test vectors that detect a fault in the dominating set will detect all the faults in the corresponding equivalent set.

For example, suppose there are N faults in a specific equivalent set and there are M faults in its corresponding dominant set. A test vector that detects a fault in the equivalent set will be able to detect all the other $N - 1$ faults in the same set. The M faults in the dominant set will also be detected by this particular test vector. Therefore, a test vector in the equivalent set can detect $N + M$ faults by the fault-collapsing technique. It requires $N + M$ test vectors to test these $N + M$ faults without fault collapsing. Hence, the number of test vectors required for fault simulating a VLSI circuit is reduced substantially by performing fault collapsing.

Test vector generation provides test vectors for a given detectable fault based on a given logic design. Several software programs are available for generating test vectors, such as the program "PODEM" written at the University of Nebraska, Lincoln [11]. The resulting test vectors are then applied to the circuit for fault simulation. The purpose of running fault simulation is to identify all detectable faults by a given test vector. The errors at the outputs of the circuit caused by a specific circuit fault with the applied input test vectors are obtained after fault simulation. By this means, a faulty transistor or connection is easily detected and in some cases located.

The output from fault simulation is fault-coverage percentage. Fault-coverage percentage is defined as the number of faults tested divided by the total number of possible faults. Usually, it is extremely difficult to achieve 100 percent fault coverage in a VLSI circuit, i.e., to detect all the possible faults. If there are undetectable faults, the designer can modify the logic design to reduce logic redundancy. Logic redundancy is the primary reason for not being able to achieve 100 percent fault coverage. Typically, it takes a long time to modify the logic design of a VLSI circuit to reduce logic redundancy. Consequently, a 98 percent fault coverage is normally acceptable for most VLSI designs [12].

IV. Design for Testability

Due to recent advancements in VLSI technology, a VLSI chip can contain hundreds of thousands of transistors. The testing of such VLSI chips has become unmanageable with conventional testing schemes, and design for testability has gained increasing importance. The purpose of design for testability is to achieve 100 percent of "observability" and "controllability" of a VLSI circuit. Observability means that a given node in the circuit is observable from the outside environment. Controllability means that a given node in the circuit is controllable from the outside environment. Design for testability techniques are divided into two categories: the ad hoc approach and the structured approach. Ad hoc techniques solve a problem for a specific design but are not applicable to all designs. Structured techniques are applicable in general but certain design rules are required by which a design is implemented. In the following, general techniques for design for testability are briefly reviewed. For a more detailed description, see [15].

A. Ad Hoc Approaches

The ad hoc approach is further subdivided into the following categories [13]:

(1) Partitioning

(2) Adding extra pins

(3) Signature analysis

The partitioning method is part of what is called the "divide and conquer" scheme. The complexity of test pattern generation and fault simulation is proportional to the number of logic gates to the third power. Therefore, it is advantageous to partition a large circuit into several smaller subcircuits and test each individual subcircuit. Figure 5 depicts a block diagram using the degating technique, which achieves circuit partition through enabling or disabling some parts of the circuit.

Adding extra pins is identical to adding test points on a VLSI chip. An extra pin can be either a primary input to enhance controllability, or a primary output to enhance the observability of the circuit. This technique is useful for small circuits only. For large circuits, the number of critical points to observe and control is large. Therefore, it is impractical to add pins to all these points due to the pin limitation.

Signature analysis relies heavily on sufficient planning in the design stage. An important part of signature analysis is a linear shift register. The outputs of these shift registers are XOR-ed to form a main output. An output taken from a node in the circuit is XOR-ed with the main output from the linear-feedback shift registers as depicted in Fig. 6. The linear-feedback shift register is initialized to the same starting place every time, and the clock sequence is a fixed number so that the test can be repeated. The circuit must also have some initialization, so that its response will be repeated as well. After steady state is achieved, the elements stored in the linear-feedback shift register are output for analysis. These elements form the signature for a "good" circuit. Thus, the result of signature analysis is simply go/no-go for the output at that particular node.

B. Structured Approaches

The structured design for testability concept is that if values in memory elements can be controlled and observed, then the test generation and fault simulation can be reduced to that of combinational circuits. The testing of combinational circuits is much easier than that of a sequential circuit and has been well developed. The structured approaches to the design for testability can be categorized into the following:

(1) Level-sensitive scan design (LSSD) [14]

(2) Scan-path design [15]

(3) Scan/set logic [16]

(4) Random-access scan [17]

(5) Self-testing and built-in testing [18, 19]

The LSSD scheme was proposed by Eichelberger et al., 1977. Some design constraints are imposed at the design stage. The LSSD design rules essentially combine two concepts that are almost independent. The first is to make the design independent of rise time, fall time, or minimum delay of the individual circuit. The only dependence is that the total delay through a number of levels must be less than some given value. This is called the level-sensitive (LS) design. The second concept is to design all the internal storage elements (other than memory arrays) so that they can also operate as shift registers. This is called the scan design (SD). The key to the LSSD design is the structure of the shift-register latch which makes the design insensitive to the outside environment. Figure 7 shows the logic diagram for a one-bit shift-register latch. In the testing mode, the shift-register latches are connected as a string. Test responses can be shifted out through the string of registers. The negative aspects of LSSD are:

(1) The latches are two to three times more complex than a conventional latch.

(2) Additional pins are required to control the shift register operation.

(3) External asynchronous input signals must not change more than once every clock cycle.

(4) All timing within the subsystem is controlled by externally generated clock signals.

The scan-path scheme is used in the design of BVD chips. It is explained in detail in Section V.

The scan/set scheme is similar to the LSSD and scan-path techniques. The basic difference is that the scan/set technique has shift registers, as in LSSD and scan-path, but these shift registers are not in the data path. Figure 8 illustrates the scan/set logic. A shift register is used both to shift in signals and shift out data. In the set function stage, signals are loaded into the shift register. These signals are fed into the system latches. The set function can also be used to control different paths to simplify the testing function. The contents of system latches can be loaded into the shift register in one clock cycle and shifted out serially. One advantage of using the scan/set technique is that the scan function can occur during system

operation since the shift register is external to the system circuit.

The purpose of the random-access scan is to have complete observability and controllability, the same as for the previous schemes. There are no shift registers needed in the random-access scan scheme. An addressing scheme which allows each latch to be uniquely selected is required instead. The addressing scheme is similar to that of a random-access memory.

Figure 9 shows the system configuration of the random-access scan network. Any point in the combinational network can be observed with some additional logic gates. Figure 10 depicts a basic type of latch (labelled "RA Latch" in Fig. 9) required in the random-access scan technique. In Fig. 10, Y_i, Q_i and CK are used in normal operation where Y_i is the output from the combinational circuit, Q_i is an input to the circuit and CK is the system clock. SDI is the scan-data input, TCK is the clock used in the testing period to scan in data, and Select i controls the ith latch to be accessed. The Select i signal is generated by decoding address inputs. By design, at most one of the Select i signals is equal to 1 at a time. Therefore, data are scanned into and out of the latches serially by a suitable combination of the TCK and Select i signals. The outputs of the RA latches are wired together since only one RA latch output is valid at a time controlled by the Select i signal.

Recently, built-in test and self-test have gained more attention. These test methods have more solid theoretical background than the ad hoc and structured approaches. The built-in logic block observation (BILBO) and syndrome testing are the two most widely used techniques for built-in and self-test. Figure 11 shows a logic diagram of a four-bit BILBO register. The BILBO register operates four modes. When B_1B_2 equals 00, the BILBO register takes on the form of a shift register. When B_1B_2 equals 10, the BILBO takes on the attributes of a linear-feedback shift register of maximum length with multiple linear inputs. When B_1B_2 equals 11, this is the normal operation with Z_i as input and Q_i as output. When B_1B_2 equals 01, the register is forced to reset. Therefore, the BILBO register can be used either as a linear-feedback shift register to generate test signals or as a pure shift register to shift data.

The syndrome testing scheme requires only minor changes to the circuit. The technique requires that 2^n patterns be applied to the n inputs of the network; the number of ones on the output are then counted. The machine faults can be detected by comparing the number of ones counted, which forms a syndrome to the circuit, to that of a good machine. However, the number of input patterns becomes prohibitively large as the number of inputs n increases.

V. The Technique of Design for Testability for BVD VLSI Chips

The scan-path scheme is adopted in the design to enhance the testability of VLSI chips for the BVD. There are two modes of operation in a scan-path design: operational mode and test mode. In the operational mode, the scan-path registers act like ordinary registers. In the test mode, all scan-path registers are connected as a single shift register. Both test patterns and test results can be shifted into and out of the chip by the shift register chain. Each scan-path register consists of a two-input multiplexer followed by a one-bit flip-flop. Figure 12 depicts the logic diagram of a scan-path register.

There are two major reasons why scan-path is chosen in the design. First, a BVD VLSI chip contains many storage elements. These storage elements can be converted into scan-path registers. Therefore, there is no need to introduce extra registers for scan-pathing. Second, quite a few I/O pins are required for a BVD VLSI chip to communicate with other components in a BVD system. Consequently, it is desirable to reduce the extra pins incurred by including the design for testability to keep the total number of pins of a BVD chip at a reasonable level. The scan-path scheme permits access to the internal nodes of a circuit without requiring a separate connection for each accessed node. One input pin for feeding in test vectors and one output pin to observe the tested results are the only extra pins required for the scan-path method. Therefore, the number of extra pins required for a scan-path access is reduced to the minimum.

The scan-path technique has several drawbacks. First, additional circuitry is added to each scan-path flip-flop. Therefore, the silicon area for a scan-path register is larger than that of an ordinary register and the chip area is increased. Second, additional chip area is needed for the scan-path interconnection since the scan-path technique requires that all the scan-path registers are connected together. Third, at least two more pins are required on the chip, the scan-input and scan-output pins. Finally, the speed of normal operation may decrease due to increased propagation delay in the scan-path flip-flops. After a thorough survey and careful evaluation of techniques used for design for testability, the scan-path scheme outperforms all the other techniques described above, despite its drawbacks.

VI. Conclusion

Because of the complexity created by the large number of gates in a BVD VLSI chip, both the fault-coverage simulation and design for testability techniques are applied to increase the possibility of success. Fault-coverage simulation can help to

detect and, in some cases, to locate the faulty components on a VLSI chip. The design for testability scheme increases both the controllability and observability of a complex chip. A tutorial on fault-coverage simulation and design for testability is given in this article. The scan-path technique is used in the BVD VLSI chip design because the area overhead incurred is small and a satisfactory performance is achieved at the same time.

References

[1] "Recommendation for Deep Space Data System Standards: Telemetry Channel Coding," (Blue Book), Consultative Committee for Space Data Systems, CCSDS Secretariat, Communications and Data Systems Division, Code TS, NASA, Washington, D.C., May 1984.

[2] R. L. Miller, L. J. Deutsch, and S. A. Butman, *On the Error Statistics of Viterbi Decoding and the Performance of Concatenated Codes*, JPL Publication 81-9, Jet Propulsion Laboratory, Pasadena, California, pp. 33–39, September 1, 1981.

[3] J. H. Yuen and Q. D. Vo, "In Search of a 2-dB Coding Gain," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 26–33, November 15, 1985.

[4] J. Statman, G. Zimmerman, F. Pollara, and O. Collins, "A Long Constraint Length VLSI Viterbi Decoder for the DSN," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 134–142, November 15, 1988.

[5] A. J. Viterbi, "Convolutional Codes and Their Performance in Communication Systems," *IEEE Trans. on Communications*, vol. COM-19, no. 5, pt. 2, pp. 751–772, October 1971.

[6] S. Arnold and F. Pollara, "A Software Simulation Study of the Long Constraint Length VLSI Viterbi Decoder," *TDA Progress Report 42-94*, vol. April–June 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 210–221, August 15, 1988.

[7] "User's Guide for the Scald Star System," Valid Logic Systems, Inc., San Jose, CA 95134, 1987.

[8] C. Mead and L. Conway, *An Introduction to VLSI System Design*, Reading, Massachusetts: Addison-Wesley, 1979.

[9] A. B. Glaser and G. E. Subak-Sharpe, *Integrated Circuit Engineering*, Reading, Massachusetts: Addison-Wesley , 1978.

[10] T. W. Williams and K. P. Parker, "Testing Logic Networks and Design for Testability," *Computer*, pp. 9–21, October 1979.

[11] P. Goel, "An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits," *IEEE Trans. on Computers*, vol. C-30, pp. 215–222, March 1981.

[12] P. H. Bardell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI*, New York: John Wiley & Sons , 1987.

[13] H. J. Nadig, "Signature Analysis, Concepts, Examples, and Guidelines," *Hewlett-Packard J.*, pp. 15–21, May 1977.

[14] S. Das Gupta, E. B. Eichelberger, and T. W. Williams, "LSI Chip Design for Testability," *Digest Technical Papers*, pp. 216–217, 1978 International Solid-State Circuit Conference, San Francisco, California.

[15] S. Funastu, N. Wakatsuki, and T. Arima, "Test Generation Systems in Japan," *Proc. 12th Design Automation Symp.*, pp. 114–122, June 1975.

[16] J. H. Stewart, "Future Testing of Large LSI Circuit Cards," *Digest Papers*, pp. 6–17, 1977 Semiconductor Test Symposium, IEEE Publication 77CH1261-7C, October 1977.

[17] H. Ando, "Testing VLSI with Random-Access Scan," *Digest Papers*, pp. 50–52, Compcon 80, IEEE Publication 80CH1491-OC, February 1980.

[18] B. Koenemann, J. Mucha, and G. Zwiehoff, "Build-in Logic Observation Techniques," *Digest Papers*, pp. 37–41, 1979 Test Conference, IEEE Publication 79CH1509-9C, October 1979.

[19] J. Savir, "Syndrome – Testing of Syndrome-Untestable Combinational Circuits," *IEEE Trans. on Computers*, vol. C-29, pp. 442–451, June 1980.

C-2

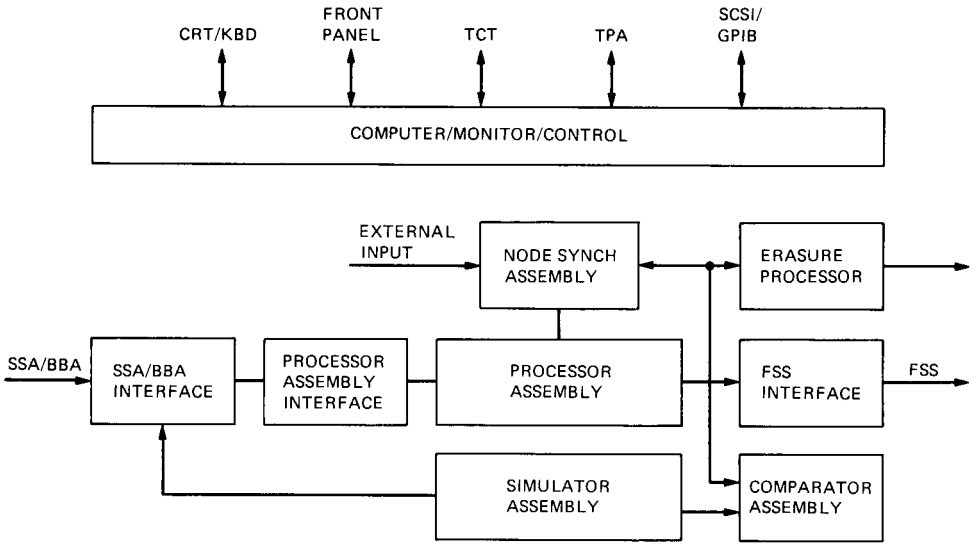


Fig. 1. Functional diagram of the Big Viterbi Decoder.

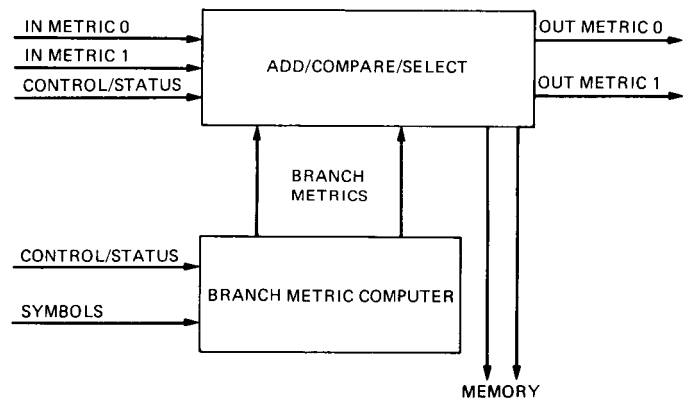


Fig. 2. Block diagram of a butterfly.

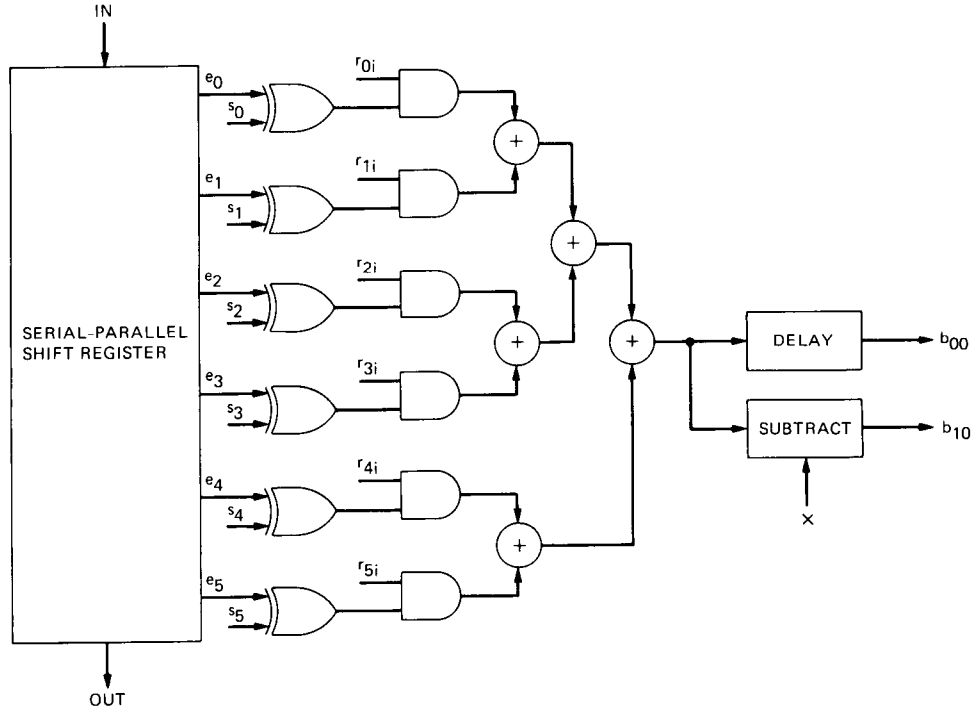


Fig. 3. Logic diagram of the branch metric computation unit.

```
 r[0]= 227 r[1]= 227 r[2]= 227 r[3]= 227 r[4]= 227 r[5]= 227
state=   0 minmetric=   0
state=   0 maxmetric=   0   bit_no=   0
p= 212 q=   0 x= 212  butt=   0  label=  0
mi0=  0 mi1=  0 mj0=  0 mj1=  0
p= 105 q= 105 x= 212  butt=   1  label= 70
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 105 q= 105 x= 212  butt=   2  label= 34
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 134 q=  56 x= 212  butt=   3  label= 44
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p=  56 q= 134 x= 212  butt=   4  label= 66
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p= 105 q= 105 x= 212  butt=   5  label= 16
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 105 q= 105 x= 212  butt=   6  label= 52
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 134 q=  56 x= 212  butt=   7  label= 22
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p=  27 q= 163 x= 212  butt=   8  label= 37
mi0=  0 mi1=  0 mj0= 27 mj1= 27
p=  56 q= 134 x= 212  butt=   9  label= 47
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p= 134 q=  56 x= 212  butt=  10  label=  3
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p=  27 q= 163 x= 212  butt=  11  label= 73
mi0=  0 mi1=  0 mj0= 27 mj1= 27
p= 105 q= 105 x= 212  butt=  12  label= 51
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 134 q=  56 x= 212  butt=  13  label= 21
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p=  56 q= 134 x= 212  butt=  14  label= 65
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p= 105 q= 105 x= 212  butt=  15  label= 15
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 105 q= 105 x= 212  butt=  16  label= 32
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 134 q=  56 x= 212  butt=  17  label= 42
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p= 134 q=  56 x= 212  butt=  18  label=  6
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p=  27 q= 163 x= 212  butt=  19  label= 76
mi0=  0 mi1=  0 mj0= 27 mj1= 27
p= 105 q= 105 x= 212  butt=  20  label= 54
mi0=  0 mi1=  0 mj0=105 mj1=105
p= 134 q=  56 x= 212  butt=  21  label= 24
mi0=  0 mi1=  0 mj0= 56 mj1= 56
p= 134 q=  56 x= 212  butt=  22  label= 60
```

Fig. 4. Output from a BVD software simulator.

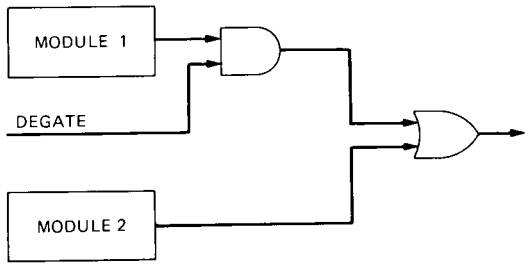


Fig. 5. Block diagram of the degating technique.

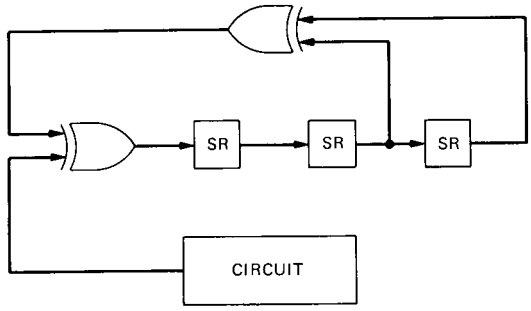


Fig. 6. Block diagram of the signature-analysis technique.

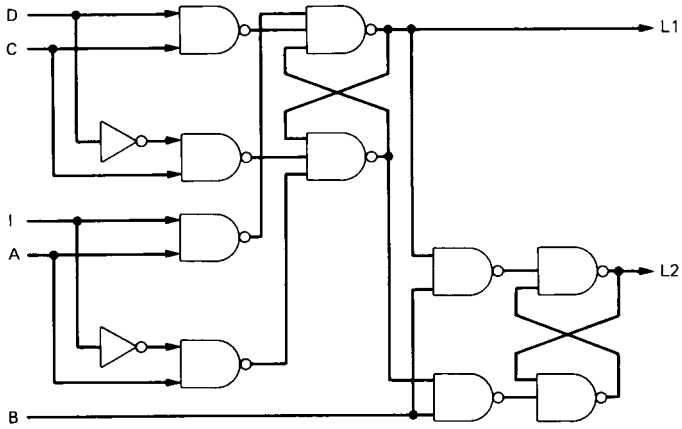


Fig. 7. Logic diagram of a one-bit LSSD shift-register latch.

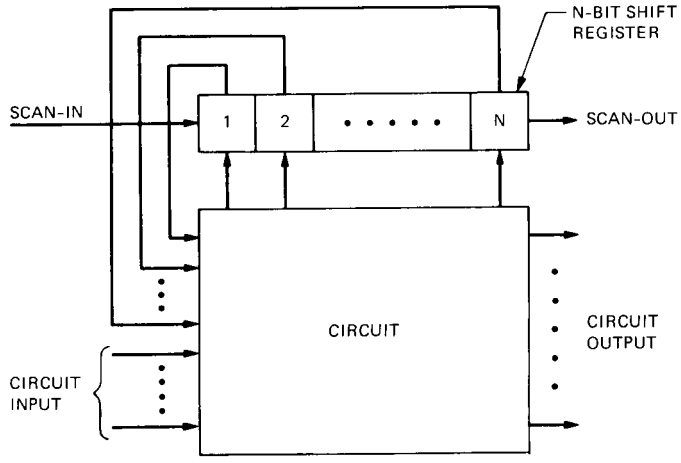


Fig. 8. Block diagram of the scan/set technique.

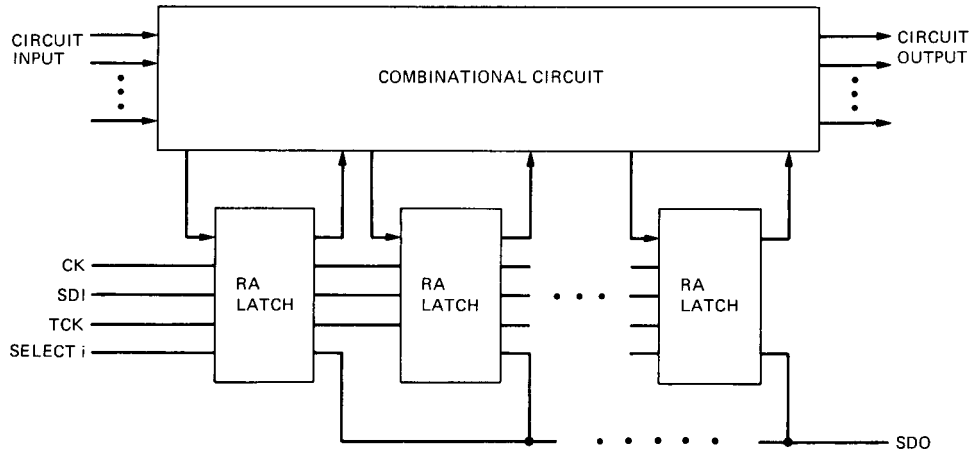


Fig. 9. Configuration of the random-access scan network.

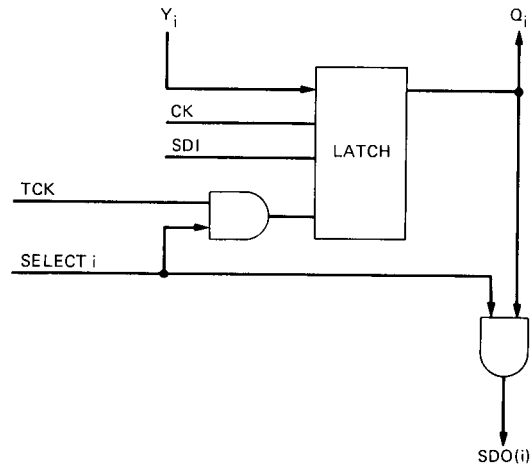


Fig. 10. Logic diagram of a random-access scan latch.

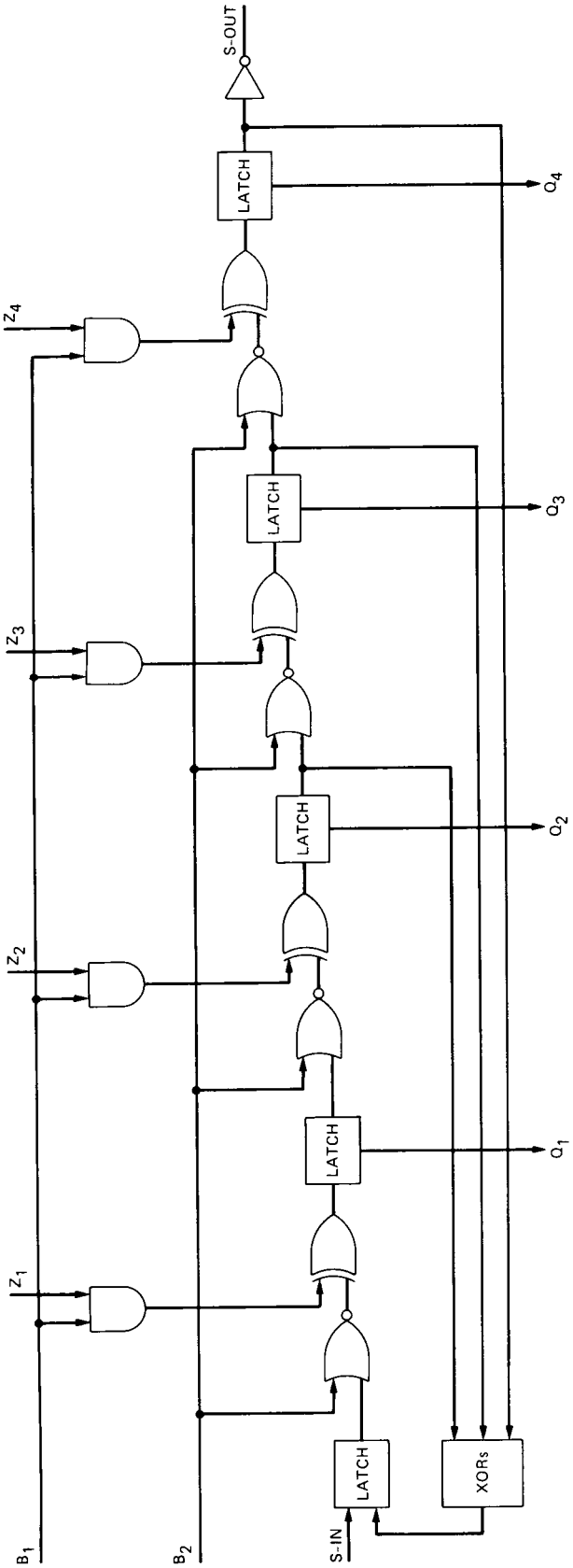


Fig. 11. Logic diagram of the BILBO technique.

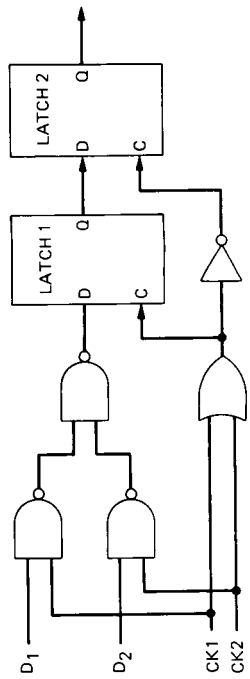


Fig. 12. Logic diagram of a scan-path register.

TDA Progress Report 42-96

October – December 1988

Wiring Viterbi Decoders (Splitting deBruijn Graphs)

O. Collins, F. Pollara, S. Dolinar, and J. Statman
Communications Systems Research Section

A new Viterbi decoder, capable of decoding convolutional codes with constraint lengths up to 15, is under development for the DSN. A key feature of this decoder is a two-level partitioning of the Viterbi state diagram into identical subgraphs. The larger subgraphs correspond to circuit boards, while the smaller subgraphs correspond to VLSI chips. The full decoder is built from identical boards, which in turn are built from identical chips. The resulting system is modular and hierarchical. The decoder is easy to implement, test, and repair because it uses a single VLSI chip design and a single board design. The partitioning is completely general in the sense that an appropriate number of boards or chips may be wired together to implement a Viterbi decoder of any size greater than or equal to the size of the module.

I. Introduction

A new Viterbi decoder [1], capable of decoding convolutional codes with constraint lengths up to 15, is under development for the DSN. This article describes a novel partitioning of the decoder's state transition diagram that forms the basis for the new decoder's architecture.

The Viterbi algorithm is naturally fully parallel [2]. However, a fully parallel implementation of a large constraint length Viterbi decoder requires an impractical amount of hardware. The first question to be faced when building such a decoder is what part of this parallelism to throw away. We decided to retain a fully distributed architecture for computing and exchanging accumulated metrics, but to perform the arithmetic computations bit-serially. The arithmetic computations are 16-bits long, so the decoding speed will be greater than 1 Mbit/sec with a 20-MHz system clock.

In a fully distributed architecture, there are 2^{K-1} basic computational elements called *add-compare-select* circuits [1] for a constraint length K decoder. When K is large, it is desirable to take a modular, hierarchical approach to organizing the huge number of required elements. Many add-compare-select circuits can be implemented on a single VLSI chip, and many chips can be mounted on a single printed circuit board. The full decoder is implemented by wiring together the required number of chips and boards.

The main problem is wiring. How can the 2^{K-1} basic elements, each with two inputs and an output (going to two different elements' inputs), be partitioned into chips and boards without using too many pins per chip or too large a board edge connector? This article shows first how pairs of add-compare-select circuits group to form elements called butterflies. The connection diagram of these 2^{K-2} butterflies is a deBruijn

graph [3]; the butterflies are nodes in the graph and the edges of the graph represent wires between butterflies. The rest of the article shows how the set of butterflies can be split into modules called boards and the boards split into modules called chips, in such a way that a large proportion of the required connections between butterflies are implemented internally within the modules. The chips are all identical and the boards are all identical. Furthermore, their internal structure does not depend on the size of the decoder, and an appropriate number of board modules and chip modules can be wired together to make a decoder of any size equal to or greater than that of the smallest module.

The constraint length 15 Viterbi decoder under development for the DSN is currently being designed with 16 boards and 512 chips. Each chip in this design contains 16 butterflies, and each board has 32 chips. However, the theory developed in this article is completely general and produces a modular, hierarchical partitioning of any size deBruijn graph into any number of first-level and second-level subgraphs (boards and chips). The exposition of the theory and the examples in this article are selected without reference to a specific configuration of the DSN's new decoder.

II. Butterflies and deBruijn Graphs

All 2^{K-1} states in a constraint length K Viterbi decoder are labeled with $(K-1)$-bit binary strings. An add-compare-select circuit takes as inputs the accumulated metrics of two states whose labels differ only in the rightmost bit. Each of these accumulated metrics has a different branch metric added to it and the smaller of the two sums is selected.

Two add-compare-select circuits take inputs from the same pair of states. The output of one of these goes to a state obtained by discarding the rightmost bit of the input states and prefixing a *0* on the left. The output of the other add-compare-select circuit goes to the state defined similarly but with a prefixed *1* instead of *0*. These two add-compare-select circuits group to form a *butterfly*, depicted in Fig. 1. The butterfly has two input wires and two output wires for transmission of accumulated metrics. The butterfly needs only four wires, because its two add-compare-select circuits get their inputs from the same pair of states. Also, it can be shown [4] that a butterfly's two add-compare-select circuits can share the same hardware for computing branch metrics. These facts make butterflies natural elements to work with.

A butterfly is labeled by dropping the rightmost bit of the label of either of its input states. The butterfly connection diagram is a deBruijn graph with 2^{K-2} nodes. Each node in this graph is labeled by a $(K-2)$-bit binary string and each edge is labeled by a $(K-1)$-bit binary string.[1] Each node is connected to four other nodes via four directed edges. A node receives its inputs via the pair of edges obtained by appending a *0* or *1* to the right of the node's label, and it sends its outputs via the pair of edges obtained by prefixing a *0* or *1* to the left of the node's label. A diagram of the connections for an arbitrary butterfly is given in Fig. 2.

III. Wiring Approaches

The full deBruijn graph of 2^{K-2} butterflies requires exactly 2^{K-1} wires for the exchange of accumulated metrics. This total number of connections cannot be increased or reduced by any wiring scheme. However, it is advantageous to capture as many of these required connections as possible within identical, small, modular units (chips and boards). Wires internal to modules can be implemented by duplicating the small module's simple wiring diagram, while external wires between modules must be implemented wire-by-wire.

One mathematically appealing way of creating identical modular units that incorporate a reasonable proportion of internal wires is to exploit one of the Hamiltonian paths [3] of the deBruijn graph. One of the two outputs of each butterfly is connected to one of the two inputs of another butterfly in a big ring (Fig. 3a). This ring contains all of the butterflies and half of their connections. The remaining half of the connections form an irregular pattern across the interior of the ring, as illustrated in Fig. 3(a). Identical modules can be constructed by slicing the Hamiltonian ring into equal-size *linear* segments (Fig. 3b). Almost half of the wires required for accumulated metric exchange can be implemented internally within the modules.

A second wiring approach is based on FFT-type connection patterns. Modules (chips and boards) are constructed from disjoint subsets of butterflies called *roots*. Each module contains its root butterflies, first-generation descendants of these roots, descendants of these descendants, and so forth. The descendants of a butterfly are the two butterflies to which it sends its outputs. The module contains all descendants at each generation except those that are roots of another module.

If a set of 2^b root butterflies is consecutive in the last b bits (i.e., the last b bits take on all possible values and all other bits are the same), then their descendants through b generations are a block of butterflies obtained by cyclic shifting the roots by b bits or less. A module containing the roots and all of

[1] In the remainder of this article, the terms *butterfly*, *node*, *butterfly label*, and *node label* will be used interchangeably, as will the terms *state*, *wire*, *edge*, *state label*, and *edge label*.

these descendants would have $(b + 1)2^b$ butterflies and the same connection pattern as an ordinary signal processing FFT of $(b + 1)$ stages, as shown in Fig. 4. This cyclic shifting may, however, generate one of the input strings. Unfortunately, it is impossible to completely partition any deBruijn graph into non-overlapping full-FFT modules. A module's connection diagram must be punctured at those nodes corresponding to root nodes of another module. The result is a *crenellated-FFT* connection pattern, a subgraph of a full FFT.

If the root butterflies are selected wisely, most of the full decoder's 2^{K-2} butterflies are found in some module's crenellated-FFT diagram. However, some butterflies do not belong to any crenellated FFT. These butterflies are *free* in the sense that their wiring is not specified by the crennellated-FFT construction. The free butterflies must physically reside within modules, but their connections to other butterflies must be implemented by external wiring (outside the modules), or else the modules' internal wiring would not be identical.

A module based on the crenellated-FFT construction thus contains two types of butterflies. The majority of butterflies belong to a crenellated-FFT pattern, and some or all of their required connections are implemented by internal wiring (within the module) which is identical from module to module. The remaining free butterflies typically have no internal connections, but instead communicate via four external pins (two for input and two for output). The pin reductions which free-butterfly interconnections make possible are trivial.

For the DSN's new Viterbi decoder, the set of root butterflies is taken to be the set of all 2^{K-4} butterflies having the common prefix *10*. This selection of root butterflies works well (i.e., captures a large fraction of wires within modules) for module sizes from 2^4 to about 2^9 butterflies.[2] The full block of root butterflies is subdivided into consecutive blocks of roots for board modules, which are further subdivided into consecutive blocks of roots for the chip modules on each board. The crenellated FFTs generated from these root butterflies are hierarchical in the sense that the crenellated FFT for the board is constructed without breaking any of the connections in the crenellated FFTs for the chips on the board.

A single shift of a string having *10* as a prefix cannot produce another string having *10* as a prefix. Hence, for modules constructed from $B_0 = 2^b$ consecutive root butterflies with the prefix *10*, the number B_1 of first-generation descendants in the crenellated FFT equals the number of roots B_0. The number of butterflies B_g in each succeeding generation, g, of the crenellated FFT is given by the linear recurrence

$$B_g = B_{g-1} - \frac{B_{g-2}}{4}$$

for $2 \leqslant g \leqslant b = \log_2 B_0$. The module only contains descendants through the bth generation; $(b + 1)$th-generation descendants cannot be included because their parent nodes belong to two different modules. It can be shown by evaluating the recursion formula that the number of free butterflies is $b + 3$ and the total number of butterflies in the module (free butterflies plus butterflies in the crenellated FFT) is 2^{b+2} or four times the number of roots. The number of external wires[3] leading off the module is $2^{b+2} + 4(b + 3)$, an average of $1 + (b + 3)2^{-b}$ external wires per butterfly on the module.

Figure 5 shows the connection diagram for a 32-butterfly chip module based on roots with the prefix *10*. The crenellated FFT is on the left and the six free butterflies on the right have all their wires leading off chip. The crenellated FFT for the chip starts with eight root butterflies and continues for three generations of descendants from these roots. The crenellated FFT resembles an ordinary 8 × 4-stage FFT, except for punctures eliminating six of the nodes. The number of external wires per 32-butterfly chip is 56.

Figure 6 shows the connection pattern for a 512-butterfly board module based on roots with the prefix *10*. The crenellated FFT contains 128 roots and 7 generations of descendants. The 128 × 8-stage ordinary FFT template is obvious, even though over half the nodes from this template are missing in the crenellated version. The crenellated-FFT structure includes 502 of the board module's 512 butterflies, leaving just 10 free butterflies per board. The number of external wires per 512-butterfly board is 552, just over 1 wire per butterfly (about half as many external wires as for a same-size module based on the Hamiltonian path construction).

Figures 5 and 6 illustrate how the definition of the first-level subgraph (a board) is completely consistent with the definition of the second-level subgraph (a chip). The 512-butterfly board in Fig. 6 is built from sixteen of the 32-butterfly chips in Fig. 5. In Fig. 6 arrows correspond to chip pins, and unconnected arrows represent board pins (which must be connected to pins on other boards via the backplane). Heavy lines represent wires on the board between chip pins,

[2] *01* would have been an equally good choice, but not *00* or *11*. Other prefixes (such as *100*) or combinations of prefixes (such as *100, 1101*) work better for larger modules. A full discussion of the efficiencies of various root selections is beyond the scope of this article.

[3] External wire and pin counts quoted in this article refer only to the wires required for exchange of accumulated metrics and do not include additional wires and pins needed for power and so forth.

and thin lines represent internal connections within the chip. Pictorially, the crenellated-FFT portions of eight of the sixteen chips in Fig. 6 are identical copies of the crenellated-FFT portion of the chip in Fig. 5, and the crenellated-FFT portions of the other eight chips are depicted by their mirror images (for convenience of display). Similarly, the depictions of the six free butterflies in each chip are displaced horizontally by varying amounts to emphasize the crenellated-FFT structure of the board.

The hierarchical nature of the crenellated-FFT construction holds not just for 32-butterfly chips and 512-butterfly boards but also for all other module sizes 2^{b+2}. Each module constructed from consecutive roots with the prefix *10* can be built from two modules half its size constructed from the same type of roots.

IV. Butterfly Addressing

Each butterfly, described by a $(K-2)$-bit binary string, must be assigned a $(K-2)$-bit address or location. The full address specifies the butterfly's exact position in the modular hierarchy. The most significant bits of the address correspond to the butterfly's board and chip location. For example, in a 2^4-board/2^8-chip configuration for a constraint length 15 decoder (2^{13} total butterflies), the four most significant bits of the address specify the board, and the next four bits specify the chip within a board. The five least significant bits of the address specify the position of the butterfly within a chip.

The addressing formula is somewhat arbitrary, but it must satisfy two basic conditions: (1) it must be a one-to-one mapping from $(K-2)$-bit butterflies to $(K-2)$-bit addresses and (2) it must be consistent with the partition of the deBruijn graph into crenellated FFTs, i.e., all butterflies assigned to certain chip and board locations by the crenellated-FFT construction should be mapped to those same locations by the addressing formula. Free butterflies may be mapped to any convenient free address.

The specification of a butterfly's $(K-2)$-bit address proceeds as follows. First, compute the butterfly's *partial address* by dropping from its $(K-2)$-bit label all of the most significant bits through and including the first occurrence of the string *10*. The partial address consists of all the bits to the right of the first *10*, and it is empty if there is no occurrence of *10* in the butterfly's $(K-2)$-bit label or if *10* first occurs in the two least significant bits. The partial address is the only part of the full address that is specified by the crenellated-FFT partition. For example, in a 2^8-chip decoder, a partial address of 8 bits will determine exactly which chip a given butterfly belongs to, but a butterfly with a partial address of 7 bits or less is one of the free butterflies that is not assigned to any chip's crenellated FFT.

The partial address sets the most significant bits of a butterfly's full address. The remaining part of the address, called *arbitrary bits*, is completely arbitrary in the sense that any choice will be consistent with the crenellated-FFT construction. However, the arbitrary bits for all butterflies must be chosen in a way that assigns each $(K-2)$-bit butterfly to a unique $(K-2)$-bit address. One simple rule for guaranteeing a one-to-one mapping is to choose the arbitrary bits as the reversal of the most significant bits (through and including the first occurrence of *10*) that were dropped to extract the partial address. Then,

$$\begin{aligned} butterfly &= (prefix, partial\ address) \\ &= (\rho(suffix), partial\ address) \end{aligned}$$

$$\begin{aligned} address &= (partial\ address, suffix) \\ &= (partial\ address, \rho(prefix)) \end{aligned}$$

where *suffix* are the arbitrary bits and *prefix* are the most significant bits of *butterfly* up to and including the first occurrence of *10*. The notations $\rho(prefix)$ and $\rho(suffix)$ denote the reversals of the indicated bit strings. For example, $butterfly = (abcde10, fghijk)$ gives $address = (fghijk, 01edcba)$, assuming that *abcde* does not contain the string *10*.

This rule produces a one-to-one mapping because it is obviously invertible. Given any $(K-2)$-bit address, first determine the partial address by dropping all of the least significant bits through and including the last occurrence of *01*. The dropped bits are the arbitrary bits. Now compute the unique butterfly label corresponding to that address by concatenating the reverse of the arbitary bits with the partial address.

V. Making Full Decoders from Chips and Boards

The board and chip modules defined by the crenellated-FFT construction have the property that full Viterbi decoders of all sizes at least equal to the size of the module can be constructed by appropriately connecting identical copies of the module, without revising the internal wiring within any module. Figure 7 shows a 32-butterfly chip wired as a constraint length 7 decoder, and Fig. 8 shows two 32-butterfly chips wired as a constraint length 8 decoder. Arrows correspond to chip pins and heavy lines represent external wires between chip pins. Thin lines represent internal connections within the chip. Note that many of the heavy lines in Fig. 8 connect butterflies within the same chip, as do all the heavy

lines in Fig. 7. However, these connections cannot be incorporated internally within the chip, because the chip would no longer be a universal module, i.e., some larger constraint length decoder could not be built from the more tightly wired chips.

VI. Bounds, Improvements, and Further Applications

There exist lower bounds [4] on the number of edges crossing cuts which divide the nodes of a deBruijn graph into sets of equal or almost equal cardinality. These follow from the very small number of short cycles in the graph and do not depend on the sets having identical internal connections. The present board design is less than a factor of two away from these bounds.

Chip and board modules may include some additional internal connections if they are destined only for a particular size of decoder (e.g., just the constraint length 15 decoder). Also, by restricting the decoder to constraint lengths 15 and larger and allowing one of the boards to be different from the others, the number of wires between boards can be reduced without changing the chips. These facts offer some flexibility if the backplane presents unexpected wiring problems.

There are additional applications for these results unrelated to building Viterbi decoders. For example, the modular decomposition of the deBruijn graph might be useful for building very big spectrum analyzers and multipliers based on the Schronager-Strassen algorithm [5].

VII. Summary

A novel partition of the deBruijn graph inspired by the problem of building a large constraint length Viterbi decoder has been introduced. The full decoder is built from identical subgraphs called boards, which in turn are built from identical subgraphs called chips. The system is modular and hierarchical, and it implements a large proportion of the required wiring internally within modules. This results in a simpler design, reduced cost, and improved testability and repairability. A constraint length 15 decoder that uses 512 identical VLSI chips and 16 identical printed circuit boards based on this partitioning is a feasible design for decoding at a speed of 1 Mbit/sec.

References

[1] J. Statman, G. Zimmerman, F. Pollara, and O. Collins, "A Long Constraint Length VLSI Viterbi Decoder for the DSN," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 134–142, November 15, 1988.

[2] R. J. McEliece, *The Theory of Information and Coding*, Massachusetts: Cambridge Press, 1977.

[3] S. W. Golomb, *Shift Register Sequences*, California: Aegean Park Press, 1982.

[4] O. Collins, *Coding Techniques for Low Signal-to-Noise Ratios*, Ph.D. Thesis, California Institute of Technology, in preparation.

[5] A. V. Aho, J. E. Hopcroft, and J. D. Ullman, *The Design and Analysis of Computer Algorithms*, Massachusetts: Addison Wesley, 1974.

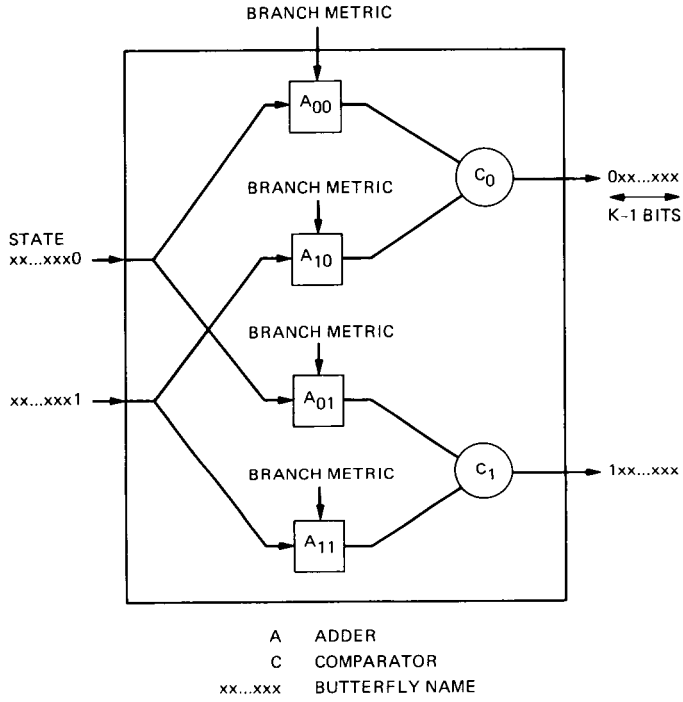


Fig. 1. The innards of a butterfly.

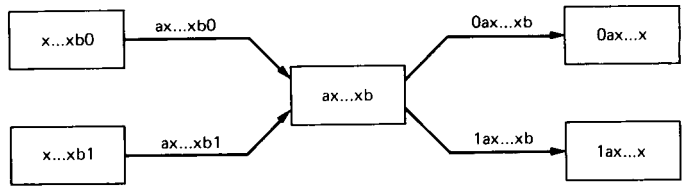


Fig. 2. Butterfly connections and labels.

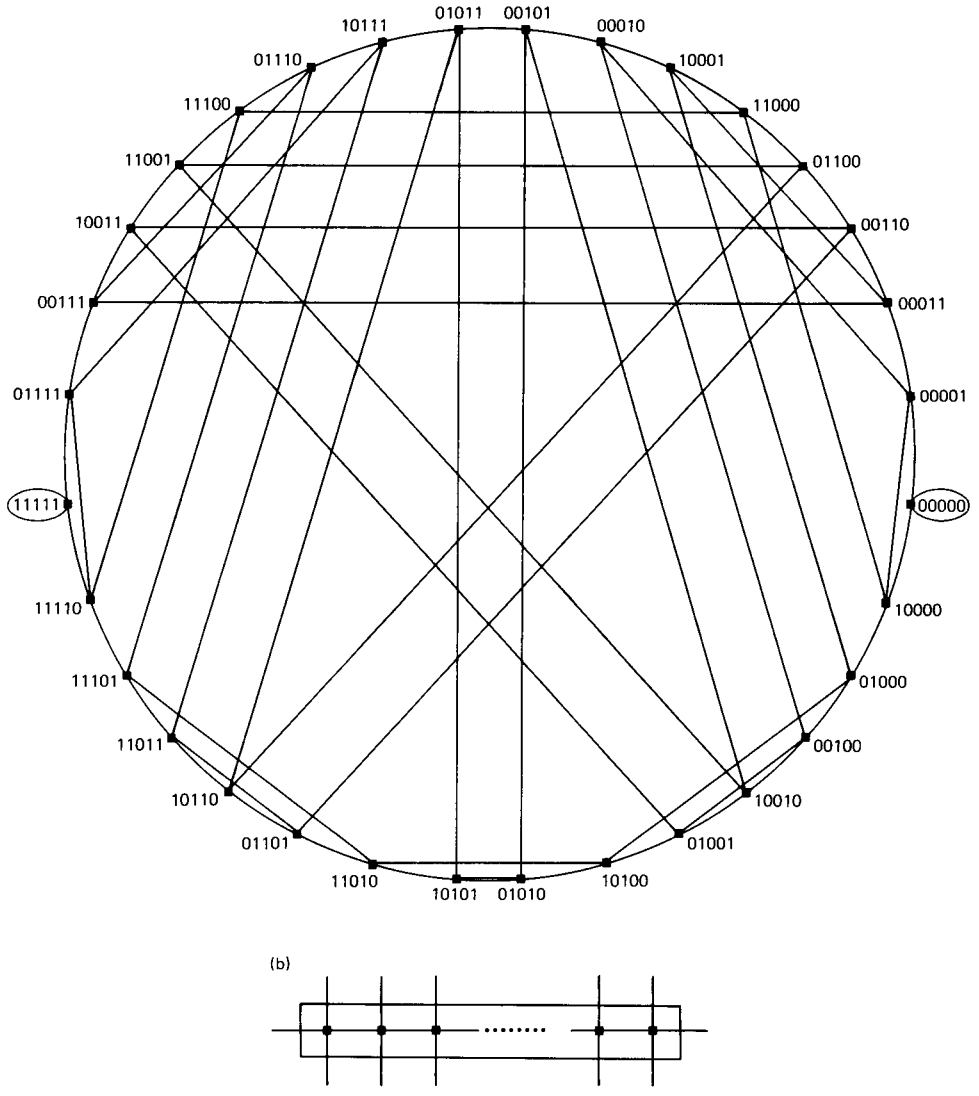


Fig. 3. (a) Butterfly connection topology for a 32-node deBruijn graph Hamiltonian path; (b) a linear module.

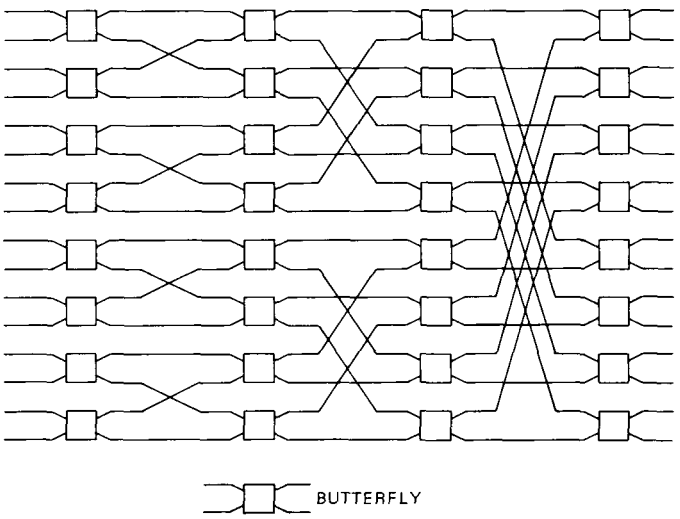


Fig. 4. Connection diagram for an 8 × 4-stage ordinary FFT.

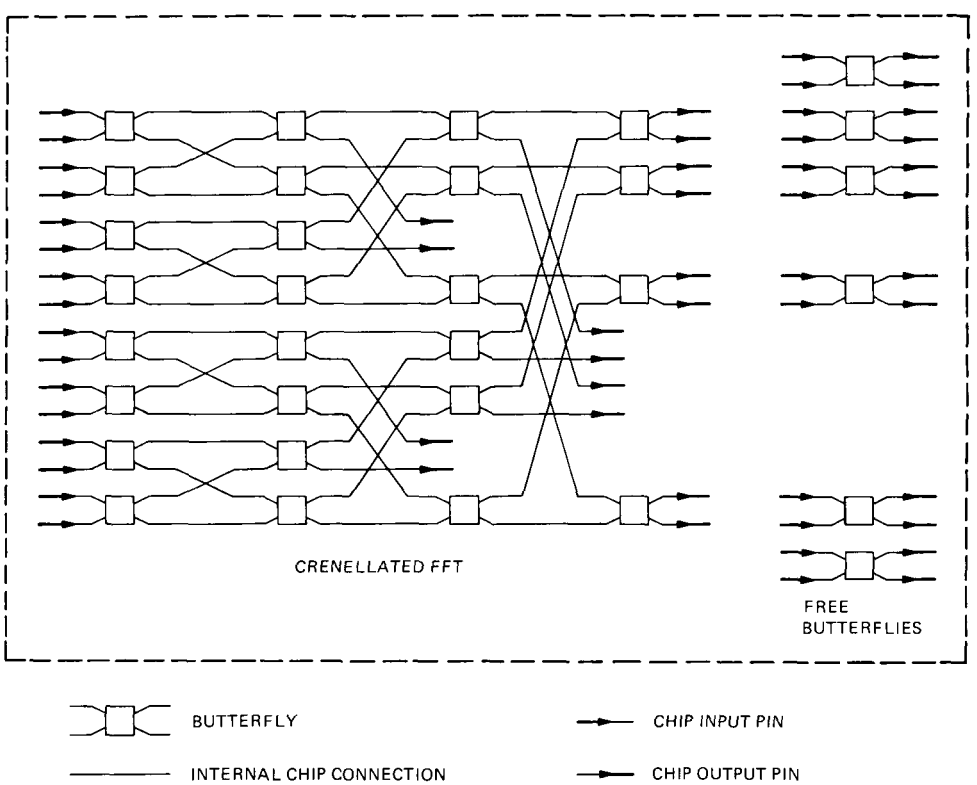


Fig. 5. Connection diagram for a 32-butterfly chip.

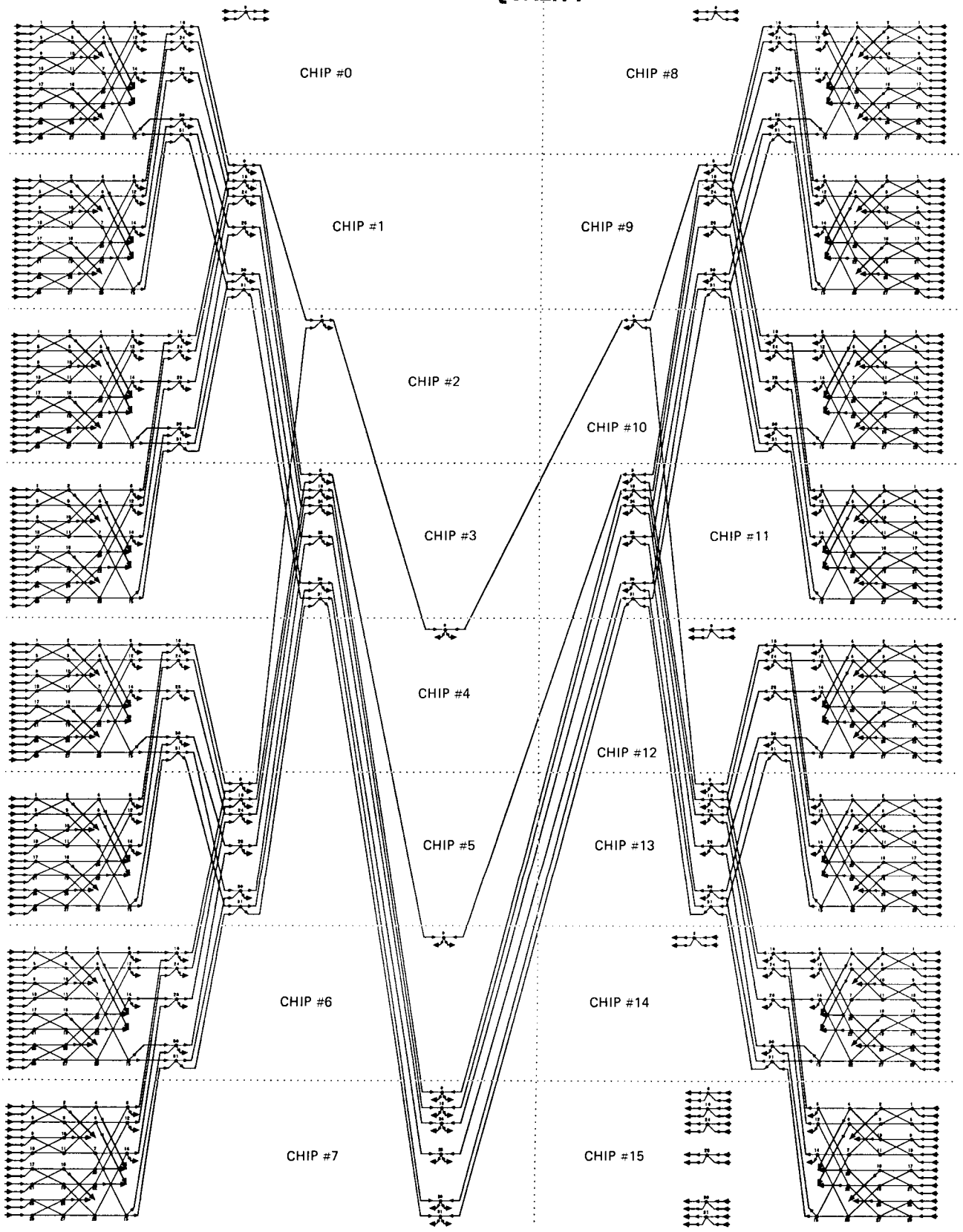
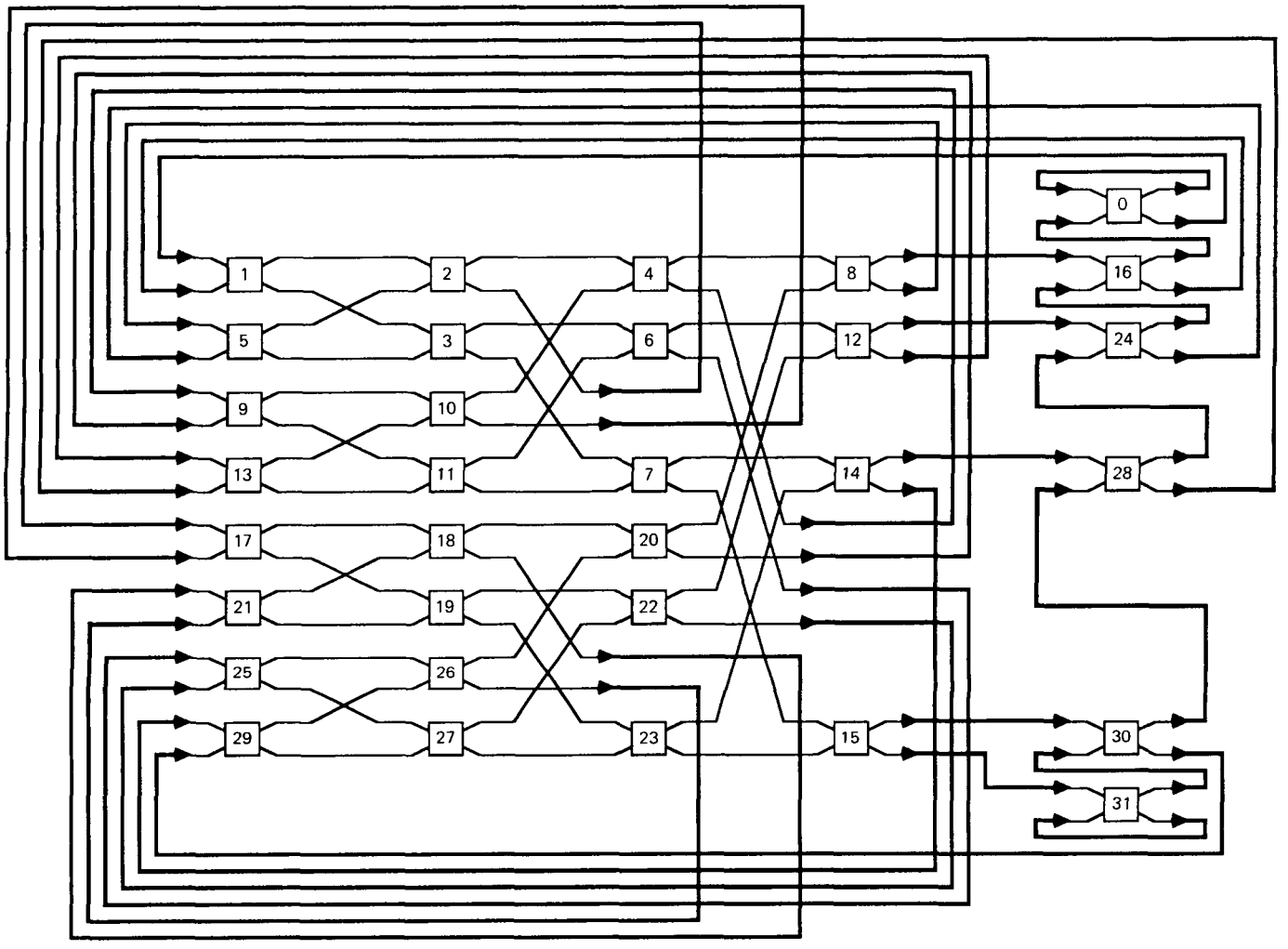
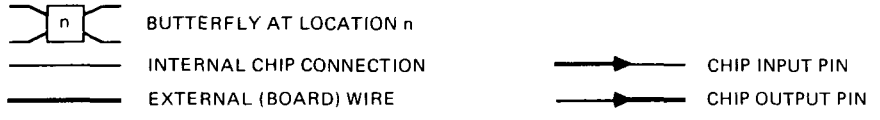


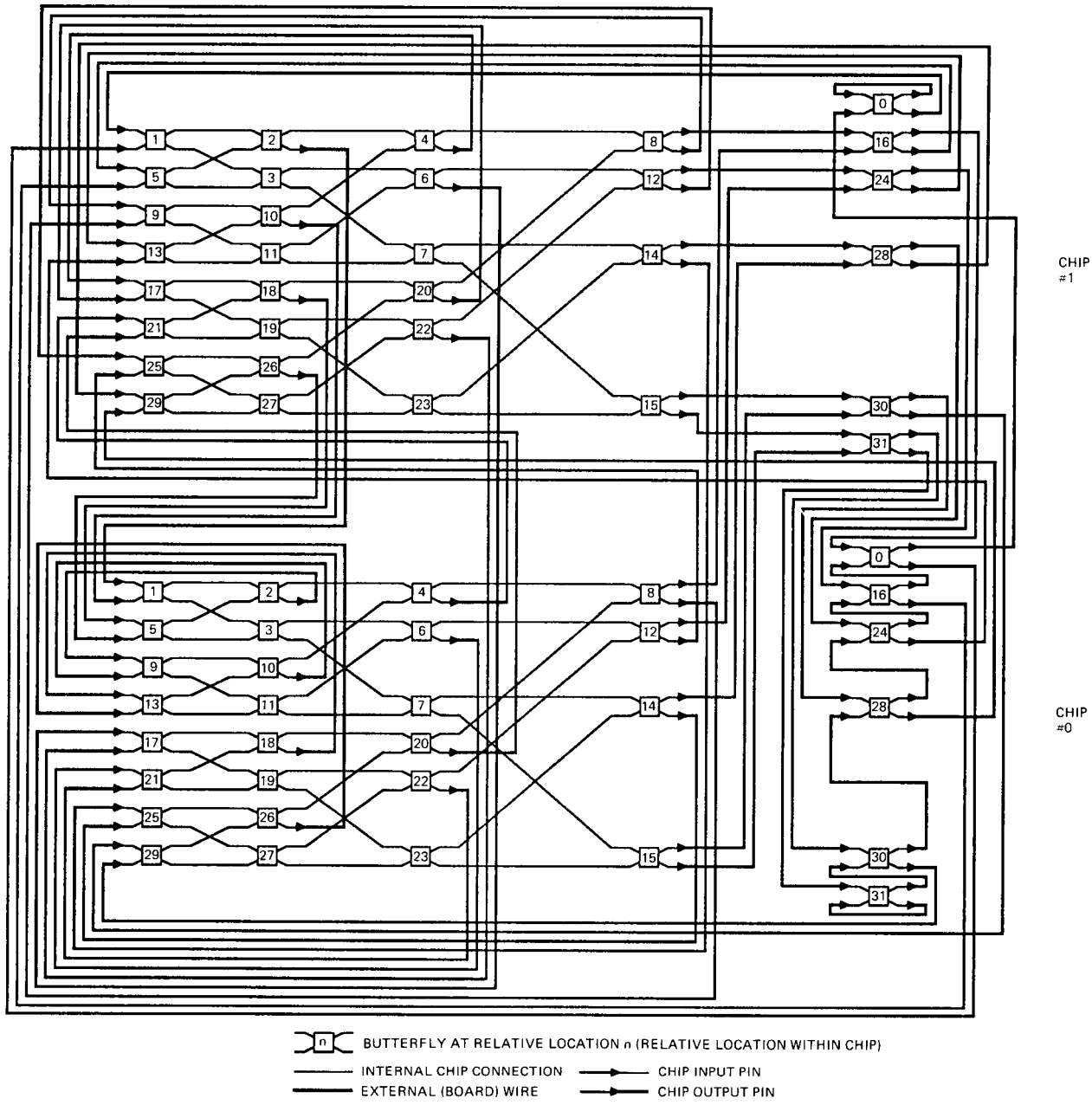
Fig. 6. Connection diagram for a 512-butterfly board.





LOCATION	BUTTERFLY	LOCATION	BUTTERFLY
0	00000	16	00001
1	10000	17	10100
2	01000	18	01010
3	11000	19	11010
4	00100	20	00101
5	10001	21	10101
6	01100	22	01101
7	11100	23	11101
8	00010	24	00011
9	10010	25	10110
10	01001	26	01011
11	11001	27	11011
12	00110	28	00111
13	10011	29	10111
14	01110	30	01111
15	11110	31	11111

Fig. 7. A 32-butterfly chip, wired as a $K = 7$ decoder.



CHIP #0

RELATIVE LOCATION	BUTTERFLY	RELATIVE LOCATION	BUTTERFLY
0	000000	16	000010
1	100000	17	100100
2	010000	18	010010
3	110000	19	110010
4	001000	20	001001
5	100001	21	100101
6	011000	22	011001
7	111000	23	111001
8	000100	24	000110
9	100010	25	100110
10	010001	26	010011
11	110001	27	110011
12	001100	28	001110
13	100011	29	100111
14	011100	30	011110
15	111100	31	111110

CHIP #1

RELATIVE LOCATION	BUTTERLY	RELATIVE LOCATION	BUTTERFLY
0	000001	16	000011
1	101000	17	101100
2	010100	18	010110
3	110100	19	110110
4	001010	20	001011
5	101001	21	101101
6	011010	22	011011
7	111010	23	111011
8	000101	24	000111
9	101010	25	101110
10	010101	26	010111
11	110101	27	110111
12	001101	28	001111
13	101011	29	101111
14	011101	30	011111
15	111101	31	111111

Fig. 8. Two 32-butterfly chips, wired as a $K = 8$ decoder.

TDA Progress Report 42-96

October–December 1988

Block Diagrams of the Radar Interface and Control Unit

J. W. Collier
Communications Systems Research Section

The Interface and Control Unit is the heart of the radar module, which occupies one complex channel of the High-Speed Data Acquisition System of the Goldstone Solar System Radar. Block diagrams of the interface unit are presented as an aid to understanding its operation and interconnections to the rest of the radar module.

I. Introduction

The Goldstone Solar System Radar contains eight radar modules. Each module processes data from a complex channel of the High-Speed Data Acquisition System [1]. The heart of each radar module is a collection of digital control circuits called the Interface and Control Unit. Because of its complexity, the interface unit is poorly understood. This article provides a systematic analysis of the interface unit through block diagrams and shows how the radar module's two main processing parameters, correlation lag length and accumulation depth, are controlled.

Understanding the interface unit's operation provides confidence in its proper operation (and by extension, confidence in overall radar processing), plus the ability to correct faults that occur in the interface unit or radar module. A further motivation occurs from time to time as the need for improved processing becomes apparent. For instance, there is a current requirement to increase the number of radar range bins from 256 to 2048. This parameter is controlled by the interface unit.

Figure 1 (from [1]) shows the functions of the radar module. Data and control signals into and out of each radar module pass through the module's Interface and Control Unit. The interface unit is commanded by a VAX 11/780 computer via a DR11-C interface, which resides on the VAX Unibus. One DR11-C serves all eight radar modules. Complex input data comes from an analog-to-digital (A/D) converter, which may include a digital integrator, at data rates up to 10 megasamples per second for each axis. The interface unit feeds this input data to one of two demodulator/correlators. Output data from each demodulator is fed directly to an accumulator. The correlation lag length and number of accumulation samples are controlled by the interface unit, and are programmable from the VAX computer. (Each radar module has four wire-wrapped boards: two demodulator/correlator boards, one board containing both accumulators, and the Interface and Control Unit board.) Output data from the accumulators go to the VAX computer through a general purpose input/output processor (GPIOP) and Floating Point Systems FPS 5210 array processor. These units are outside the radar module. An overview of the entire radar processor is given in [2].

II. Demodulator/Correlator and Accumulator Functions

The digitized radar echo signal, corrupted with noise, is correlated with a delayed version of itself or with a locally generated version of the maximal length pseudorandom noise

(PRN) code which was transmitted. In each case, the correlation is between a four-bit representation of the signal and a single-bit representation of either the delayed signal or PRN code.

Let the signal data be divided into n sets, with each set consisting of 256 samples. Then the ith sample from the nth data set is

$$S(i,n) = s_3(i,n) \cdot 2^3 + s_2(i,n) \cdot 2^2$$

$$+ s_1(i,n) \cdot 2^1 + s_0(i,n) \cdot 2^0$$

where each s_i is either a 1 or 0, and $i = 0, 1, \ldots, 255$.

The output of the correlator/demodulator at instant i, using 256 lagged values of $S(i,n)$, is

$$Y(i,n) = \sum_{k=0}^{255} S(i-k,n)\,C(k,n)\,M(k)$$

$$n = 0, 1, 2, \ldots \qquad (1)$$

where $C(k,n)$ is binary-valued, and represents either the most significant bit of the signal $S(k,n)$ or the PRN code. The $M(k)$ represent binary-valued mask bits (properly called "unmask" bits) used to prevent undesired terms from appearing in the sum. The mask bits set the upper value of the summation index if fewer than 256 terms are desired, that is,

$$M(k) = 1 \;, \quad k = 0, 1, \ldots, m \leqslant 255$$

$$M(k) = 0 \;, \quad m < k \leqslant 255$$

Each $Y(i,n)$ occupies a time bin, i.e., a radar range bin. There are 256 bins in each radar module. Since the correlator/demodulator sums 256 samples, each containing four bits, each $Y(i,n)$ occupies 12 bits.

The Y are further filtered at the accumulator by summing values from different sets, $n = 0, 1, 2, \ldots$, with the same subscript i. The summation can occur for up to 2^{16} sets. If the number of accumulations of each term is N_a, then the output of the accumulator, after N_a additions, is an array of 256 terms with each term given by

$$A(i) = \sum_{n=0}^{N_a-1} Y(i,n) \;, \quad i = 0, 1, \ldots, 255 \qquad (2)$$

where

$$1 \leqslant N_a \leqslant 2^{16}$$

Since up to 2^{16} values of $Y(i,m)$, each 12 bits wide, are summed, the $A(i)$ occupy 28 bits.

A new array of accumulator outputs is available for every $256N_a$ samples at the input of the demodulator. For 10^7 samples/sec and $N_a = 65535$, this occurs at approximately 1.68-sec intervals.

In the evaluation of Eqs. (1) and (2), three cases are of interest, depending on the nature of the $C(k,n)$ factor in Eq. (1).

A. Case 1: Autocorrelation

In Case 1, the received signal is correlated with itself.

$$C(i,n) = s_3(i,n)$$

$$M(i) = 1, \quad i = 0, 1, \ldots, 255$$

$$1 \leqslant N_a \leqslant 2^{16}$$

The transmitted signal is a continuous wave. $C(i,n)$ is the most significant bit of the returned signal. All demodulator lags are unmasked. The number of accumulations can be any value from 1 to 2^{16}.

In the second and third cases, the received signal is cross-correlated with the PRN code which generated the transmitted signal.

B. Case 2: Cross-Correlation with Long Code

The PRN code length $L > 256$. Then N_a is set to approximately $L/256$ [3], as illustrated in Fig. 2(a). The $M(i)$ mask bits are set to 1 for all 256 values of i. This maximizes the correlation between received signal and locally generated code. (This assumes that the code has been correctly delayed to make signal and code line up. This is done through the polynomial-driven time base and PRN generator module outside the radar module, and a software loop.)

C. Case 3: Cross-Correlation with Short Code

The PRN code length $L \leqslant 256$. Then, N_a is set to 1, corresponding to one accumulation in Eq. (2), as shown in Fig. 2(b). The $M(i)$ are set to 1 for the duration of the PRN code word.

The actual implementation of Eqs. (1) and (2) is as follows:

The mask bits $M(k)$ are serially loaded into four correlators. After loading, they remain stationary. Each bit of the signal and the single code bit are serially loaded into one of the correlators, at the signal sample rate (<10 megasamples/sec). At each sample instant, the correlation $Y(i, n)$ is computed.

In order to maintain a running partial sum for the ith value of the summations, the accumulators must store 256 values of $Y(i)$, which grow to 28 bits. Therefore, the accumulator must have a 256 X 28 memory for each set of $A(i)$, and data must be stored and retrieved at the signal sample rate. There are separate memories for the I and Q channels. In addition, the GPIOP reads the data from one set, while a new set is being formed. Therefore, the accumulator board has four memories with 256 X 28 bit capacity, and read/write access time capable of handling 10-megasample/sec data.

The interface unit also contains a memory which is used to provide test data, plus mask and code bits for the two demodulators. Each demodulator requires four bits of data, plus one mask bit and one code bit for 256 lag positions. Therefore the memory size is 256 X 12 for the two demodulators. Although this memory is loaded by the relatively slow DR11-C, it must be downloaded to the demodulators at the signal sample rate.

III. Interface and Control Unit Operation

Figures 3, 4, and 5 present details of the interface unit in block diagram form. The drawings show considerably less detail than the 10-page Radar System Interface Unit schematic.[1] Concentration here is focused on bussed data, important signals, and clusters of circuit elements. For instance, groups of integrated circuit counters are condensed to single blocks, and all integrated circuit packages have been reduced to five types: three-state buffers, registers, counters, multiplexers/demultiplexers, and random-access memory. The details of combinational gating, often a hindrance in understanding controllers, appear as notes on the block diagrams.

A. Interface with DR11-C

Figure 3 shows the connections between the DR11-C and the interface unit. The DR11-C interface consists of two 16-bit unidirectional busses named OUT ⟨0:15⟩ and IN ⟨0:15⟩. At the interface unit, the signals pass through three-state buffers. The busses are accompanied by the following control signals [4]:

CSR0, CSR1. These are user-programmable bits supplied by the DR11-C, used here to select whether DR11-C data is written to Broadcast Register in each interface unit or written to/read from Function Register in the selected interface unit.

INIT. Indicates Unibus reset.

ODTRAN. Same as DR11-C's Data Transmitted. This is a 400-nsec positive pulse indicating that the DR11-C has received data FROM the interface unit. The trailing edge is used.

ONDRDY. Same as the DR11-C's New Data Ready. This is a 400-nsec positive pulse indicating that the DR11-C has transmitted data TO the interface unit. The trailing edge is used.

Each of the eight interface units contains eight Function Registers which can be written from, or read by, the DR11-C interface. Thus the DR11-C must be able to address 64 locations.

A 16-bit Broadcast Register in each interface unit is programmed with a pointer which selects the interface unit and the Function Register to be written or read (see [5]).

The DR11-C has two user-defined bits, CSR0 and CSR1. When CSR0, CSR1 = 00, the data from the DR11-C bus is written to the Broadcast Register. When CSR0, CSR1 = 10, data is written to the Function Register pointed to by the Broadcast Register. (The other two combinations for CSR0, CSR1 are presently unused.) The formats of these eight registers plus the Broadcast Register (from [1]) are shown in Fig. 6.

The particular interface unit (one of eight units) is selected by a three-bit subfield in the Broadcast Register, while the Function Register (one of eight registers) is selected by another three-bit subfield.

The unit address is decoded to form a signal called MODEN (Module Enabled). MODEN gates either the write or read signal from the DR11-C (ODTRAN or ODTRDY) to a demultiplexer/decoder, to form a set of clocks called $\overline{\text{RDFR}n}$ and $\overline{\text{CKFR}n}$ where n is a digit from 0 to 7. (A bar is used in a signal name to indicate that it is active in the zero- or 0-state.)

The $\overline{\text{CKFR}n}$ clock writes data from the DR11-C bus to Function Register n in the enabled interface unit. The clock is a negative-going pulse with 400-nsec width, which is determined by ONDRDY. Writing takes place on its trailing edge for most of the Function Registers.

The $\overline{\text{RDFR}n}$ clock reads data from Function Register n, and gates this data to the DO bus. It is a negative-going pulse with 400-nsec width, which is determined by ODTRAN. The data is placed on the bus while $\overline{\text{RDFR}n}$ is at a low level.

[1] Radar System Interface Unit Schematic (internal document), Communications Systems Research Section, Jet Propulsion Laboratory, Pasadena, California, June 22, 1987.

B. Interface with Demodulator

Figure 4 shows how the interface unit controls the demodulator. Signal data for the demodulator comes from the A/D converters, or may be simulated from test data stored in a random-access memory in the interface unit. The signal data consists of four bits plus a one-bit code bit (or "reference bit"). The single code bit is either the MSB of the unshifted signal or the pseudonoise code.

A system clock (SYSCLK) is supplied from the A/D to the interface unit, which relays it to the correlators and to the accumulators.

The mask bits $M(i)$ from Eq. (1) are downloaded by the DR11-C to the interface unit's memory, and downloaded from there to the correlators where they are stored. They only need be downloaded to the demodulators once for a particular set of lags.

Function Registers 0 to 4 (see Fig. 6) specify the sources for the correlator signal and code bits. Function Register 0 uses bits 0 to 7 to point to the current memory address, and bits 8 and 9 to specify whether the address is to be incremented after a memory read or write.

Data is written to memory using an address counter clocked by CKBM (Load Addresss Counter, Fig. 4). The memory is preloaded with a starting address, using bits 0 to 7 from the DR11-C bus when $\overline{\text{CKFR0}}$ is active. If $\overline{\text{CKFR0}}$ is active, data is written to Function Register 0. (In other words, the counter is Function Register 0, at least for bits 0 to 7.) The counter output assumes this value until a positive-going clock edge is received at CKBM.

Referring to the first note in Fig. 4,

$$\overline{\text{CKBM}} = (\overline{\text{FR008}} + \overline{\text{RDFR1}}) * (\overline{\text{FR009}} + \overline{\text{CKFR1}})$$

both $\overline{\text{RDFR1}}$ and $\overline{\text{CKFR1}}$ are negative-going pulses which occur whenever a memory read/write operation occurs. Therefore, CKBM has a positive-going transition only if FR008 or FR009 (which are bits 8 and 9 of function register 0) is true.

Bits 0, 1, and 2 of Function Registers 2 and 3 determine whether the correlator data or mask or code are loaded from memory or from the A/D unit. IBE and QBE (which are derived from these three bits) select a path from the A/D units or from memory (Fig. 4).

If correlator data is to be dumped from memory, then IBE and/or QBE is active and the memory is read at the system clock rate and transmitted to the correlators. Data can also be dumped from memory back to the DR11-C by reading Function Register 1, which enables buffers (Fig. 3). Reading occurs at the address loaded into the Load Address Counter.

C. Interface with Accumulators

Figure 5 shows how the interface unit controls the accumulators. One accumulator has been shown in some detail so the reader can see how the control signals are used.

Twelve-bit data words enter the accumulator at the system clock rate. The accumulator has two 28 X 256 memories for each axis, designated A and B. Partial sums (which can grow to 28 bits in length) for each demodulator lag time are stored in one memory, while complete sums are read from the other memory by the GPIOP. This double-buffering requires external circuitry which is housed in the interface unit. Each memory's address is controlled by an address counter, which is periodically preloaded with all zeros. The interface unit controls the clocking of this counter (which occurs at the system clock rate) and the load time, and selects which counter and which side of the double-buffer are enabled.

The maximum memory address is determined by the maximum lag length in the demodulator. This data is loaded into Function Register 4 (Fig. 5). Eight bits are used for each demodulator. The maximum accumulation length is set in Function Register 5 for I data and 6 for Q data.

These registered values are compared with counters which are preset to zero. Since address-stepping must occur at the incoming data rate from the demodulator, a counter (Fig. 5) is clocked at the system clock rate.

When the counter outputs equal the registered values, another data set of partial sums has been completed. This event clocks another counter which tracks the number (denoted N_A) of data sets. A D-flip-flop with a delay element feedback creates a pulse for this secondary clocking. These counters are compared with a preloaded value of N in Function Registers 5 and 6.

The four comparator output signals, plus CKFR7 and RDFR7 and the system clock, create the necessary control signals. The circuits involve a number of combinational and synchronous gates which are too complex to generalize here. The outputs of the combinational block consist of four sets of signals, one set for each address counter on the accumulator board (Fig. 5).

Accumulator output data is fed to the GPIOP. The device address, as seen from the GPIOP, is determined by an 8:1

multiplexer arrangement, similar to the one used with the DR11-C interface (compare Figs. 3 and 5).

IV. Functional Testing of the Interface and Control Unit

The programmable features of the demodulators and accumulators (in particular, the correlation length and number of samples to be accumulated) are controlled by the interface unit. A simple test is proposed here to ensure that these controls work properly.

The test consists of moving an impulse function through each of the radar module's 256 range bins. An impulse can be created by correlating a maximal-length ($\leqslant 255$) pseudonoise sequence code with itself at the demodulator input. Such a code is available at the output of the polynomial-driven time base and PRN generator which is housed in another part of the radar processor [6]. Alternately, the code can be loaded into the interface unit's memory.

The conceptual test setup is shown in Fig. 7. The programmable delay is set to produce a delay kT_s where T_s is the sample period of data at the input of the correlator, and k ranges from 0 to 255. (This delay is programmable at the coder's control registers.)

At the output of the accumulator, the autocorrelation is

$$R_x(t) = -a \qquad t \neq kT_s$$

$$= La \qquad t = kT_s$$

where a is a scale factor, and L is the length of the PRN sequence.

The test can be made quite vigorous by "exercising" each part of the radar module separately. Suppose, for instance, that range bins at one end of the 256-bin range have unexpectedly low values using real data for long range codes (corresponding to Case 2 described in Part II). Assuming that a test impulse also exhibits the same problem, then the accumulation number N_a can be set to different values, beginning with zero. According to Eq. (2), the output impulse (which is actually observed at the output of the FPS 5210 array processor) should increase linearly with N_a at the affected bin. Failure to do so would isolate the accumulator as the source of the problem, or possibly the part of the interface unit which controls the accumulator's address counters. If the signal did increase linearly, but had different values than for other bins, then the problem lies in the demodulator or its controls in the interface unit.

The mask bits can be used to turn the impulse on or off. This verifies that the interface unit's memory and address counters are working properly.

Finally, the test can be used to prove performance for a longer lag length, and under any desired operating condition. It could also be expanded to include the baud-integrating A/D converters which precede the radar module.

V. Summary

This article has presented block diagrams of the Interface and Control Unit, a digital processor that controls functions inside the radar module and provides interconnections between the module and the outside world.

A simple test was proposed which completely verifies operation of the interface unit controls. This test can be further expanded to verify operation under different configurations.

References

[1] S. S. Brokl, "Controller and Interface Module for the High-Speed Data Acquisition System Correlator/Accumulator," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 113–124, November 15, 1985.

[2] L. J. Deutsch, R. F. Jurgens, and S. S. Brokl, "The Goldstone R/D High-Speed Data Acquisition System," *TDA Progress Report 42-77*, vol. January–March 1984, Jet Propulsion Laboratory, Pasadena, California, pp. 87–96, May 15, 1984.

[3] E. Satorius and S. S. Brokl, "Goldstone Solar System Radar Performance Analysis," *TDA Progress Report 42-93*, vol. January–March 1986, Jet Propulsion Laboratory, Pasadena, California, pp. 302–308, May 15, 1988.

[4] DR11-C General Device Interface User's Manual, Publication EK-DR11C-OP, Digital Equipment Corporation, Maynard, Massachusetts.

[5] S. S. Brokl, "A General Monitor and Control Interface to the VAX Unibus by Way of DR11-C I/O Port," *TDA Progress Report 42-83*, vol. July–September 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 125–133, November 15, 1985.

[6] K. H. Farazian and R. F. Jurgens, "Programmable Digital Baud Integrator for the Radar High-Speed Data Acquisition System," *TDA Progress Report 42-79*, vol. July–September 1984, Jet Propulsion Laboratory, Pasadena, California, pp. 142–151, November 15, 1984.

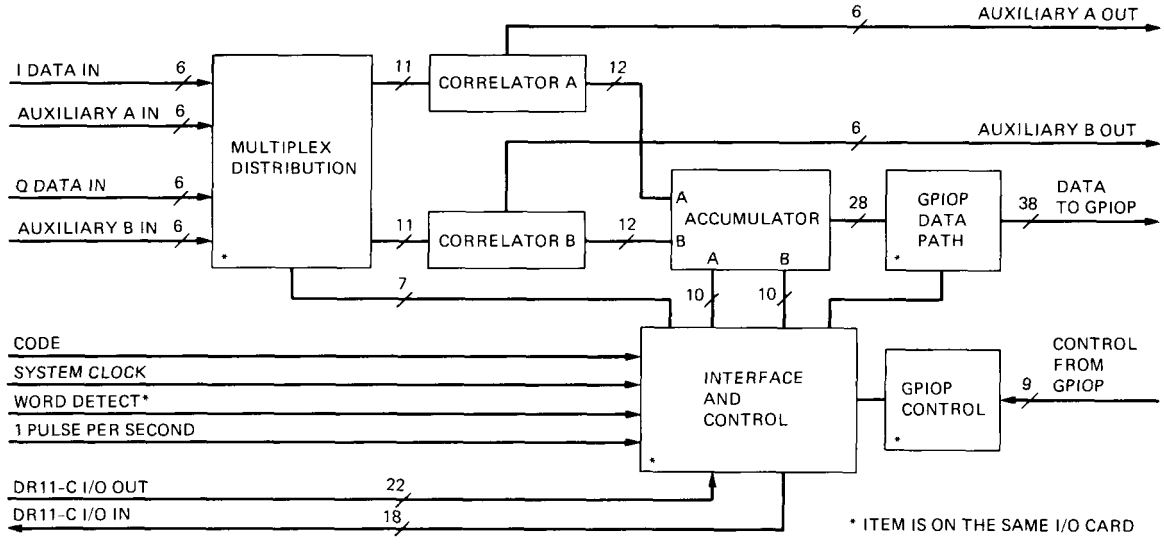


Fig. 1. Radar module block diagram.

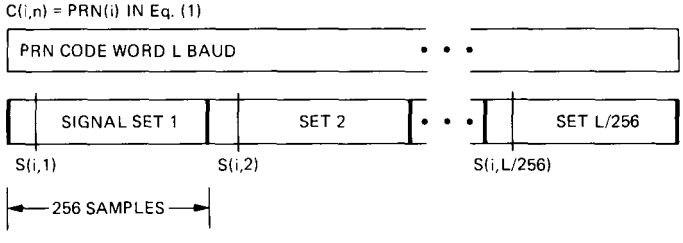


Fig. 2(a). Cross-correlation with long code.

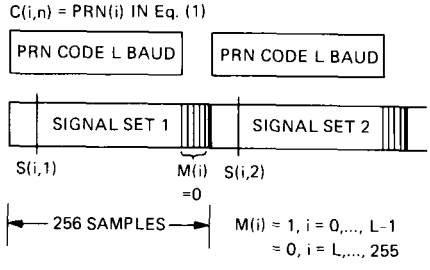
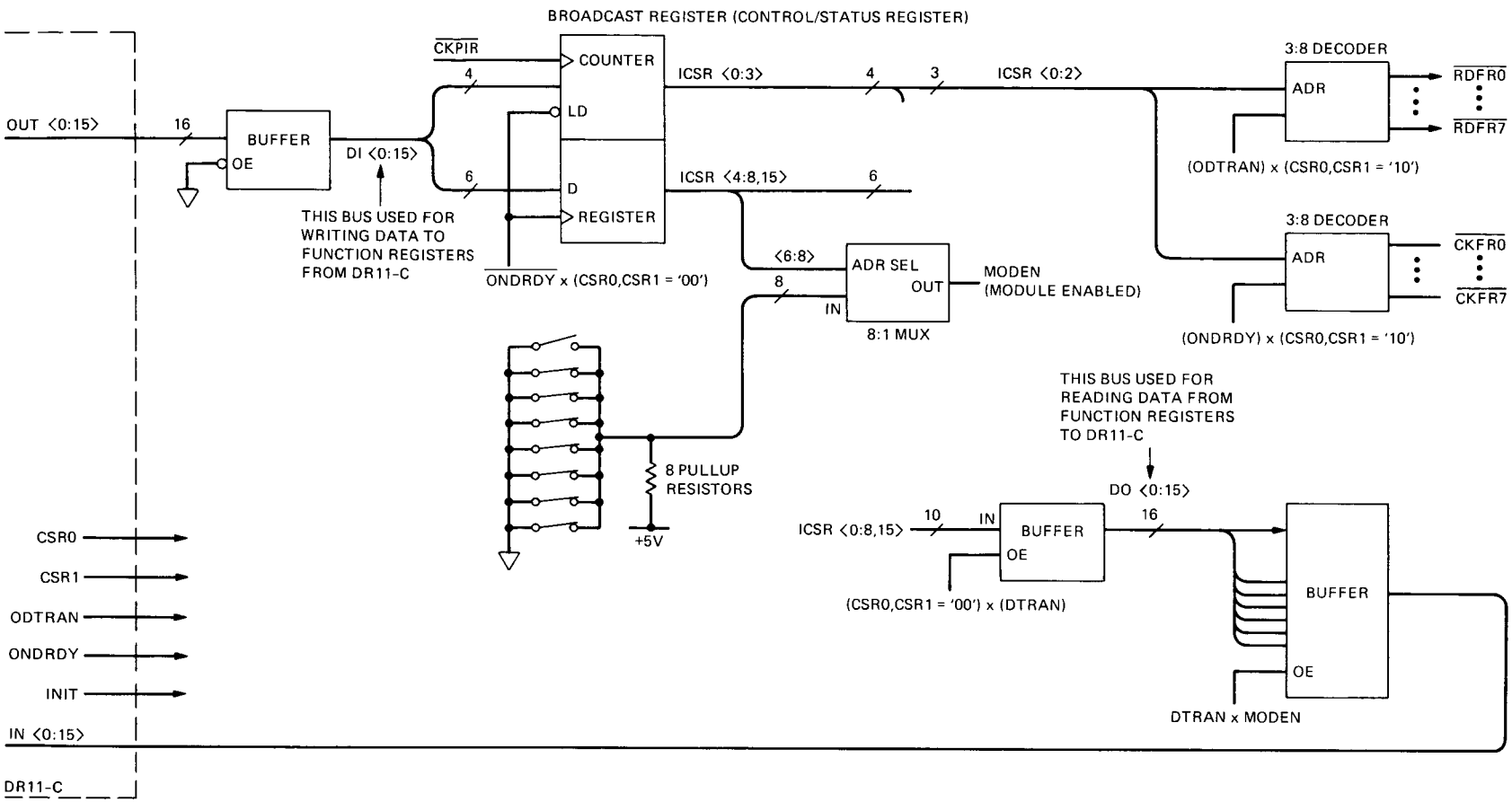


Fig. 2(b). Cross-correlation with short code.



$\overline{CKPIR}$ = (FR008 + $\overline{ICSR04}$ + $\overline{ODTRAN}$) * (FC009 + $\overline{ICSR05}$ + $\overline{ONDRDY}$)

FR008,FR009 = BITS 8,9 OF FUNCTION REGISTER 0

(THE INTENT IS TO INCREMENT FUNCTION REGISTER POINTER IF ICSR04 OR ICSR05 = '1', BUT TO INHIBIT THIS IF FR008 OR FR009 IS '1'.)

Fig. 3. Block diagram of interface with DR11-C.

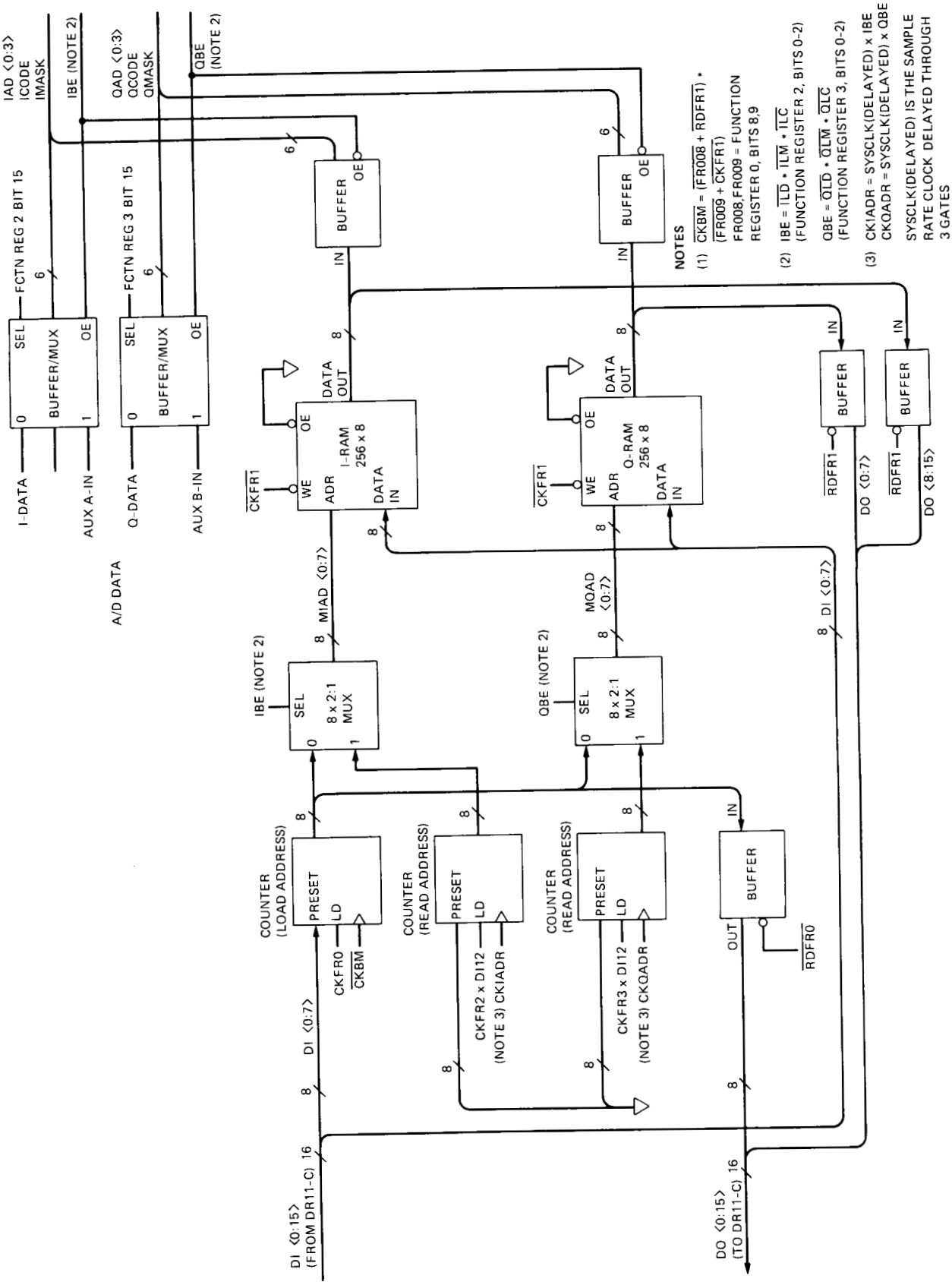


Fig. 4. Block diagram of interface with demodulator.

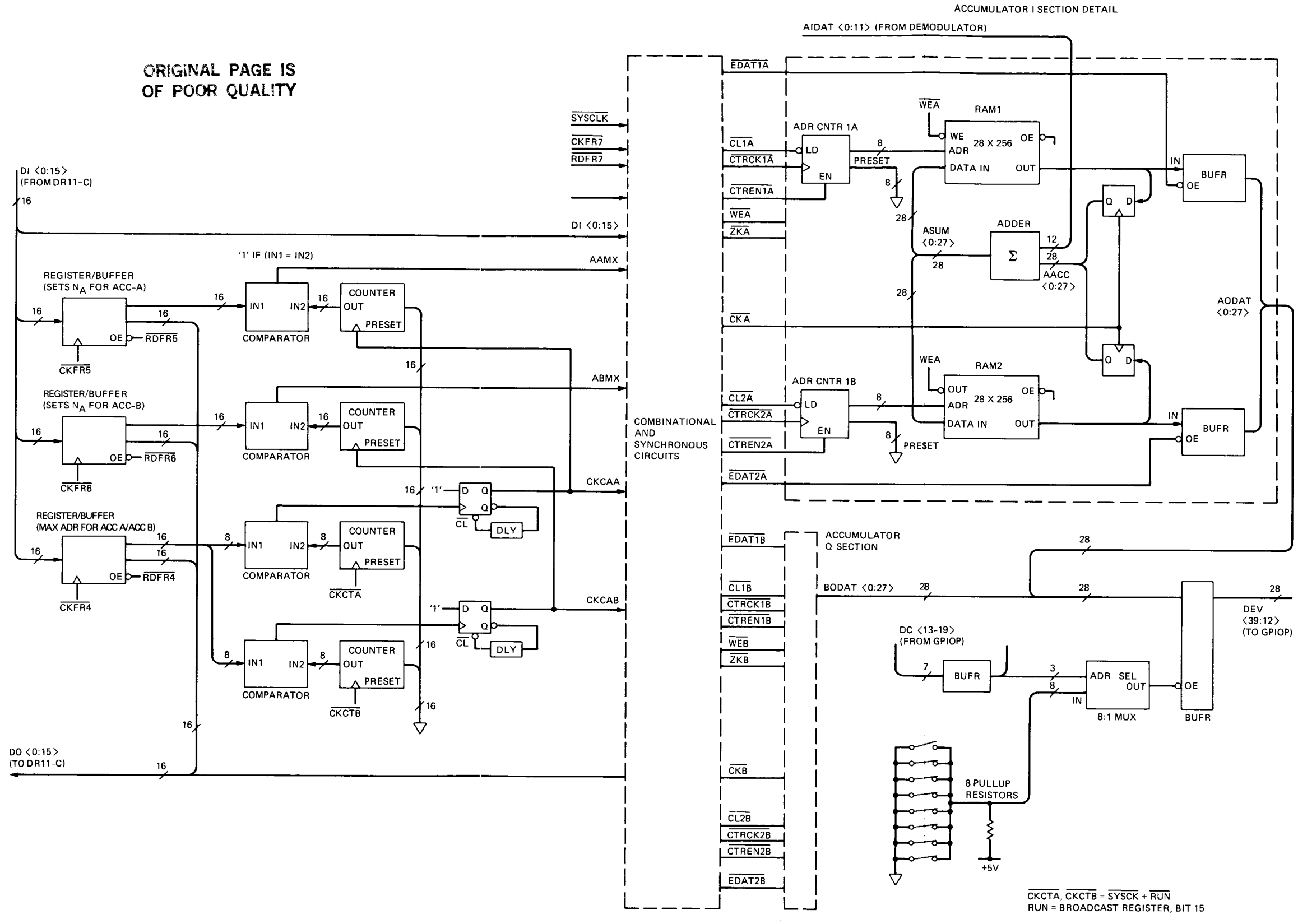


Fig. 5. Block diagram of interface with accumulator.

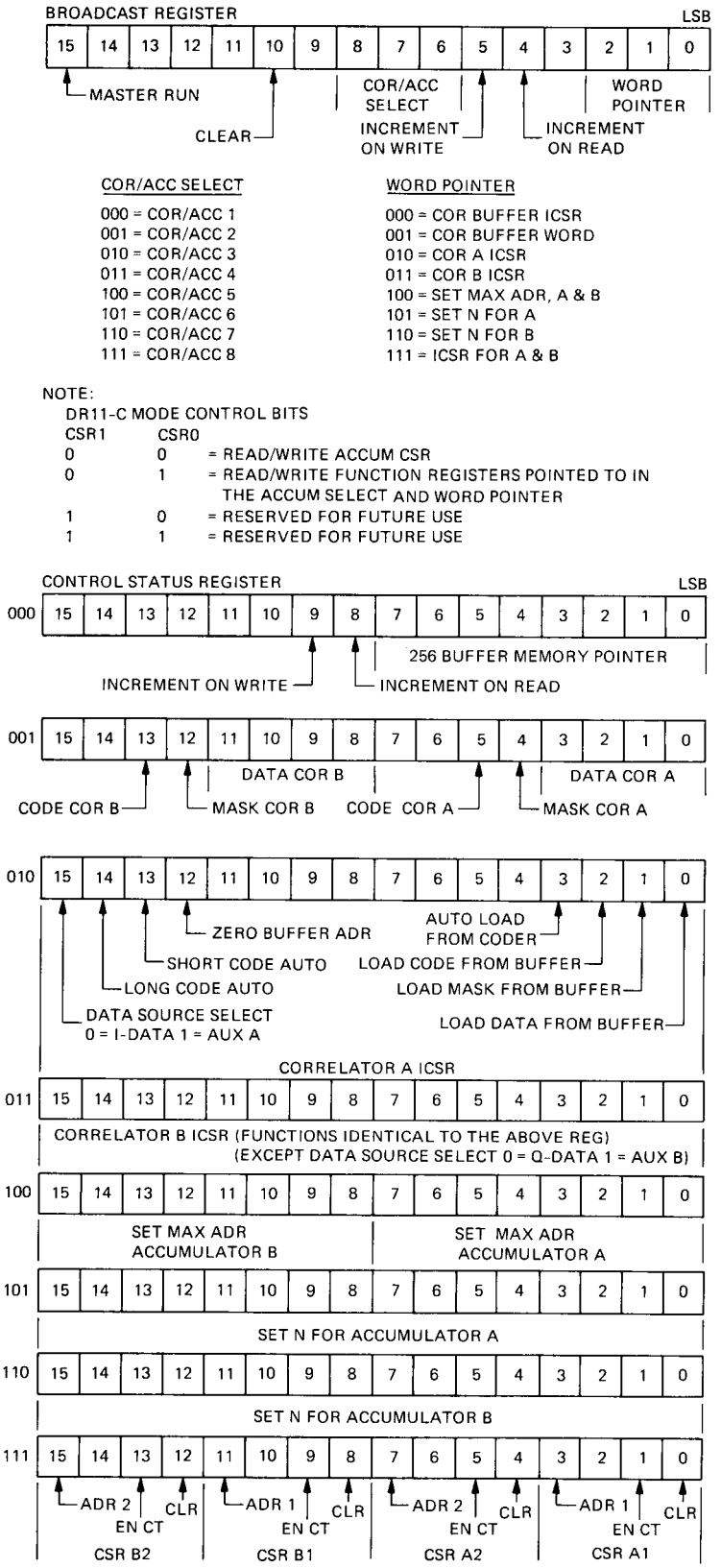


Fig. 6. Interface and Control Unit Function Registers.

PRECEDING PAGE BLANK NOT FILMED

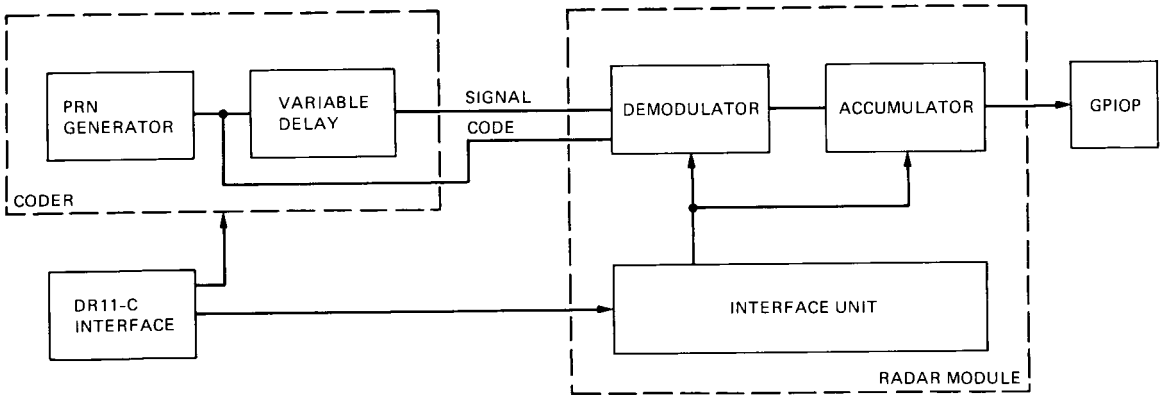


Fig. 7. Setup for radar module test.

RF Performance Measurement of the DSS-14 70-Meter Antenna at C-Band/L-Band

M. S. Gatti
Ground Antenna and Facilities Engineering Section

A. J. Freiley
Radio Frequency and Microwave Subsystems Section

D. Girdner
TDA Mission Support and DSN Operations

The calibration of the 70-meter antenna at C-band (5.01 GHz) and L-band (1.668 GHz) is described. This calibration comes after a modification to an existing L-band feed to include the C-band frequencies. The test technique employs noise-adding radiometers and associated equipment running simultaneously at both frequencies. The test procedure is described including block diagrams, and results are presented for efficiency, system temperature, and pointing.

I. Introduction

For three separate days in October 1988, the RF performance of the 70-meter antenna at DSS-14 was measured. The measurements were done at L-band (1.668 GHz, $\lambda = 17.98$ cm) and C-band (5.01 GHz, $\lambda = 5.98$ cm) to evaluate the efficiency and pointing of the system. The measurements were performed using radiometric techniques with observations of a selected set of celestial radio sources.

The existing L-band feed on DSS-14 [1] has been recently modified to include C-band uplink for support of the Phobos mission. The C-band uplink is designed to handle maximum power of 15 kilowatts, while the L-band channel is receive only. The new C-band feed consists of a disc-on-rod antenna which is located in the center of the existing L-band horn. Future reports will describe the detailed design of the C-band feed [2]. The location of the L/C-band feed on the antenna is such that the phase centers are not located on the focal ring, but are instead located approximately 24 inches from the focal ring. This results in a scanning of the secondary pattern beams from the nominal boresight of the antenna. Both C- and L-band beams are coincident, i.e., they point in the same direction. A significant point of interest is that since the C-band feed is not optimally located, there is a considerable performance degradation from a typical DSN antenna. A preliminary analysis [3] indicated that this configuration will provide satisfactory performance, which the tests described here confirm.

II. Measurement Methodology

The methodology chosen for calibration of the antenna at these frequencies follows closely the techniques used in past programs [4, 5]. Celestial radio sources of known flux densi-

ties, noise-adding radiometers, and azimuth-elevation tracking are used to determine performance. The specific techniques are described below.

A. Radiometric Techniques

The technique used to measure the performance of the antenna was to employ a noise-adding radiometer (NAR) [6], which is standard equipment for calibration of DSN antennas. The system noise power from the feed is combined with modulated noise power from a noise diode, downconverted to an IF signal, and detected with a square-law detector. The square-law detector output is transmitted to the NAR computer and display unit, a BP-80 in this case, which demodulates the signal and calculates Y-factor ratios from which the system noise temperature is computed. In addition, manual Y-factors at the RF frequency were measured and correlated with the NAR with good success. Receiver linearity is always a concern in systems with large dynamic ranges, and was taken into account for these measurements.

B. Measurements

As stated earlier, the objectives of the test were to evaluate the efficiency of the antenna, the system temperature, and pointing at each frequency. These performance measurements of the antenna were made simultaneously at the L- and C-band frequencies.

To measure the efficiency of the antenna, a celestial radio source is acquired and the rise in system noise temperature with respect to the off-source temperature is recorded. The actual measurement sequence consisted of measuring the boresight beam direction, measuring the system temperature when the antenna beam was pointed on source and off source, and performing NAR calibration approximately every hour. This was performed many times during the course of the observation period, i.e., the source was tracked across the sky while continuously moving the beam on and off source. During the course of tracking across the sky, each radio source would move in elevation, first rising, the setting, all the while increasing in azimuth. Therefore, tracking required that the antenna vary in elevation as a function of the time of the track. The result is measurement in efficiency as a function of elevation for each on-off pair. This was performed for several sources, which are listed in Table 1.

The equivalent off-source system temperatures T_{op} as a function of elevation angle are a by-product of the efficiency measurements. The locus of values T_{op} versus elevation (called a tipping curve) are provided, as well as zenith T_{op}.

The antenna was boresighted periodically to update and maintain correct pointing of the antenna beam. A boresight consists of bisecting the beam at the 3-dB points to determine the beam direction. This was done by using a standard strip-chart recorder and commanding the antenna to proceed or follow the source by a fixed angle. The difference in the off-peak levels is balanced manually via appropriate commands to the antenna control system, and the elevation and cross-elevation data is recorded. The offset determined by this measurement is then entered into the antenna pointing system to complete the pointing update.

C. Radio Sources

The sources used for this calibration program included 3C274 (Virgo A), 3C84 (Perseus A), 3C123, 3C295, and 2134+00. The source information and characteristics (flux density, position, etc.) were provided by the Space Physics and Astrophysics Section. Table 1 shows the information assumed for these measurements. The efficiency of the antenna under test is calculated by the ratio of the measured on-off antenna temperature change ΔT_a to the source 100 percent efficiency temperature. The source 100 percent efficiency temperature is related to the flux density of the source S, the physical area of the antenna A_p, and Boltzmann's constant k, and is given by

$$T_s(100\%) = \frac{SA_p}{2k} \tag{1}$$

Note that Table 1 also provides information for source resolution correction C_r. The efficiency therefore is given by

$$\eta = \frac{\Delta T_a}{T_s(100\%)} C_r \tag{2}$$

Of this list of sources, only 3C274 is considered a calibration standard source. This means that the value of $\Delta T_a(100\%)$ in Table 1 for other sources may be significantly in error due to variability; however, these sources are steady enough during the course of a day's observation that relative information may be obtained. Then, by comparing the efficiency for other sources with 3C274 at a common elevation angle, a systematic correction can be determined. At the end of the testing, these corrected source temperatures were provided to the Space Physics and Astrophysics Section as a data point in their database regarding the variability of the source with time. In this way, by observing many sources at different elevation angles, a complete chart of efficiency versus elevation can be generated.

III. Antenna Configuration

A block diagram of the measurement configuration is shown in Fig. 1. A discussion of this configuration follows.

A. Feed/Transmission Lines

The feed is mounted on the side of the XRO feedcone with the waveguides penetrating the cone to connect to the low-noise amplifiers (LNAs). The position of the feed is such that the phase center is located approximately 24 inches outside the focal ring. The L-band waveguide contains an L-band low-pass filter, couplers for signal injection and sampling, and a waveguide switch. The waveguide switch allows either the feed or an ambient load to be connected to either of the two LNAs. The C-band waveguide also contains couplers, a switch and ambient load, and the capability for water cooling.

B. Receiver

The L-band receiver used in these measurements consisted of the L-to-S upconverter and operational Block IV receiver. The IF signal from the receiver was tapped into at the alidade where the NAR instrumentation was located. This allowed for a complete calibration of the L-band system and minimized additional cable runs.

The C-band system normally operates as transmit only, therefore, an R&D receiver was installed temporarily until the operational calibration receiver could be delivered. The receiver used was the same one used to perform calibration tests of the feed at the Microwave Test Facility (MTF) at Goldstone.

C. Other Instruments

Other instruments that completed the measurement system included the noise diodes, located in the cone, a JPL-designed BP-80 NAR, square-law detectors, noise-diode controllers, power meters, filters, and spectrum analyzers. The noise-diode controllers were used both as modulators of the noise-diode sources in the cone, and as on/off switches for the diodes for use in receiver linearity checks. The spectrum analyzer was used to view the receive band of frequencies for RFI, which was at times a serious problem. When RFI was present, appropriate filters at the IF frequency were used.

IV. Test Results

A. Pointing/Subreflector Positioning

The pointing data acquired in these tests not only aided in defining the antenna efficiency, but also provided data to better define the total errors of the 70-meter pointing system. Pointing data from measurements of any feed position also provide information in the ongoing iterative process of blind pointing improvement.

For pointing, a datum must be chosen from which pointing may be referenced. This datum is a model of how the antenna performs given many different input parameters such as gravity, preset elevation and azimuth offsets, etc. For these tests, the datum consisted of a model derived from calibration data taken in mid-August 1988 on the XKR feedcone, referred to here as the XKR model. The pointing model for this feedcone was selected because the pattern of this X-band feed is the narrowest. The location of the L/C-band feed is known with respect to the XKR feedcone; therefore, predictions regarding the beam pointing were made and only those parameters changed in the model. All data were taken from this initial L/C-band pointing model. Offsets in the actual beam pointing from the direction of the model were measured during the course of observations. All offsets measured fell within +5 to −3 millidegrees in elevation and within −2 to −7 millidegrees in azimuth cross-elevation. The small size of these offsets indicates that the initial L/C-band pointing model is fairly accurate.

The original model for the L/C-band antenna was updated as a result of these tests and the elevation and cross-elevation beam pointing directions are shown in Table 2. The pointing directions in Table 2 reflect the latest updates due to this sequence of tests. In this table, column 2 shows the position of the XKR radar beam (the datum), column 3 shows the position of the C-band, and column 4 shows the delta between the XKR and C-band. Columns 5 and 6 are for L-band positions and deltas. The last column shows the pointing difference between the C-band and L-band beams.

B. System Noise Temperature

The intrinsic noise temperature of the antenna at both C-band and L-band was measured using two separate techniques. The first technique consisted of a manual Y-factor measurement of the RF signal using a tuned RF receiver (TRF) which consisted simply of a post-LNA amplifier, bandpass filter, isolator, and power meter. The second technique was to use the NAR instrumentation as discussed above. In both of these techniques, the results agreed to within a few percent. Also, an analysis of the configuration was done to estimate the noise temperature. The actual and predicted values for the zenith T_{op} are given in Table 3. Table 4 gives the various components that make up the predicted values of T_{op}.

In addition, the system temperature as a function of elevation was measured during the course of the efficiency calibration. These data for C-band are given in Fig. 2, and for L-band in Fig. 3. Shown in these figures are the composite data for all days' observations. Also shown on both of these curves are data resulting from tipping the antenna in elevation while measuring the system temperature. This curve is highlighted by the solid line.

C. System Gain/Efficiency

The system gain is calculated by multiplying the efficiency by the maximum theoretical gain which is given by

$$G_{100} = \left(\frac{\pi D}{\lambda}\right)^2 \quad (3)$$

where D = the antenna diameter (70 meters), and λ = the operating wavelength. The measurement of the system efficiency is obtained from Eq. (2) given in Section II. Like the tipping curve, the efficiency is given as a function of elevation, due to the motion of the radio source across the sky. The efficiency versus elevation for C-band is given in Fig. 4, and for L-band in Fig. 5.

D. Receiver Linearity

Linearity may be a problem for receivers that are expected to operate across a large dynamic range. The large dynamic range of the NAR is required because the on-source/off-source signal levels are often quite different. In addition, the calibration of the NAR uses an ambient load which is a factor of 5 to 10 times increase in power over the system noise power. To assure that the receiver is producing the correct results, a technique of systematically adding a small excess noise to the measurement is used. This noise is added to the signal during calibration, when the system temperature is near 350 K, and then during off-source noise measurement, when the system temperature is near 100 K. If the system is linear, the value of excess noise added at each end of the dynamic range will be the same. Any required corrections follow the techniques developed earlier [7] and consist of fitting a second-order equation to the results of four measurements of the following:

(1) Ambient load plus the excess noise

(2) Ambient load

(3) Antenna plus excess noise

(4) Antenna

From the second-order fit, corrections may be applied to subsequent measured data.

V. Conclusions

The 70-meter antenna has been upgraded to include C-band transmit by modifying the existing L-band feed. Calibrations of the C-band and L-band feed were presented including efficiencies, system temperatures, and pointing. It is noted that the antenna beams are offset from the nominal boresight axis due to the lateral displacement of the feed. The antenna efficiency is therefore lower than could be achieved if the subreflector was moved to a more optimum position. This is a possible area of improvement if required in the future. The measurements provided valuable pointing data which may be used as baselines for other pointing calibrations.

References

[1] J. Withington, "DSN 64-Meter Antenna L-Band (1668-MHz) Microwave System Performance Overview," *TDA Progress Report 42-94*, vol. April–June 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 294–300, August 15, 1988.

[2] P. Stanton, "The L/C-Band Feed Design for the DSS-14 70-Meter Antenna (Phobos Mission), in preparation, Jet Propulsion Laboratory, Pasadena, California.

[3] D. Hoppe and P. Stanton, "Calculated 70-Meter Antenna Performance for Offset L-Band and C-Band Feeds," *TDA Progress Report 42-90*, vol. April–June 1987, Jet Propulsion Laboratory, Pasadena, California, pp. 12–20, August 15, 1987.

[4] A. J. Freiley, "Radio Frequency Performance of DSS 14 64-Meter Antenna at X-band Using an Improved Subreflector," *TDA Progress Report 42-60*, vol. September–October 1980, Jet Propulsion Laboratory, Pasadena, California, pp. 168–176, December 15, 1980.

[5] A. J. Freiley, "Radio Frequency Performance of DSS 14 64-m Antenna at X-Band Using a Dual Hybrid Mode Feed," *DSN Progress Report 42-53*, vol. July–August 1979, Jet Propulsion Laboratory, Pasadena, California, pp. 132–139, October 15, 1979.

[6] P. D. Batelaan, R. M. Goldstein, and C. T. Stelzried, "A Noise-Adding Radiometer for Use in the DSN," *JPL Space Programs Summary, 37-65*, vol. II, Jet Propulsion Laboratory, Pasadena, California, pp. 66–69, 1970.

[7] C. T. Stelzried, "Non-Linearity in Measurement Systems: Evaluation Method and Application to Microwave Radiometers," *TDA Progress Report 42-91*, vol. July–September 1987, Jet Propulsion Laboratory, Pasadena, California, pp. 57–66, November 15, 1987.

Table 1. Celestial radio source list for C- and L-band calibrations

Radio source	Position, R.A., 1950 Dec, 1950	L-band			C-band		
		Flux density, jansky	T_s, 100%, kelvin	Source resolution correction, C_r	Flux density, jansky	T_s, 100%, kelvin	Source resolution correction, C_r
3C274	12:28:17.6 +12 40 01.7	183.99	256.44	1.2	71.89	100.2	1.19
3C84	07:16:29.6 +41 19 51.9	52.77	73.542	1.0	48.49	67.584	1.0
3C123	04:33:55.2 29 34 14.0	42.38	59.061	1.001	16.48	22.970	1.0099
3C295	14:09:33.5 +52 26 13	19.19	26.747	1.0	6.36	8.865	1.0
2134+00	21:34:05.1 00 28 27.0	8.28	11.54	1.0	9.18	12.801	1.0

Table 2. Pointing directions of the C- and L-band antenna

Parameter	XKR radar beam position, mdeg	C-band, mdeg	ΔC-band, mdeg	L-band, mdeg	ΔL-band, mdeg	ΔC to L, mdeg
Cross-elevation	−11.5	145.9	134.4	155.6	144.1	+9.7
Elevation	+14.8	−79.7	−64.9	−81.5	−66.7	−1.8

Table 3. Measured and predicted zenith system noise temperatures

Band	Tuned RF receiver, K	Noise-adding radiometer, K	Prediction, K
L-band	35.3	35.7	40
C-band	121	116	124

Table 4. Summary of elements making up the zenith T_{op} prediction

Component	Symbol	L-band value, K	C-band value, K
Feed	T_f	8.15	26.64
Transmission line	$T_{w/g}$	3.75	5.90
Spillover	T_s	7.8	11.1
Quad-leg scattering	T_{qs}	2.6	2.6
LNA temperature	T_m	12.0	71.5
Follow-up amplifier temperature	T_f	1.0	1.0
Atmosphere	T_{atm}	2.0	2.5
Galactic temperature	T_{gal}	2.7	2.7
Total	T_{op}	40.0	123.94

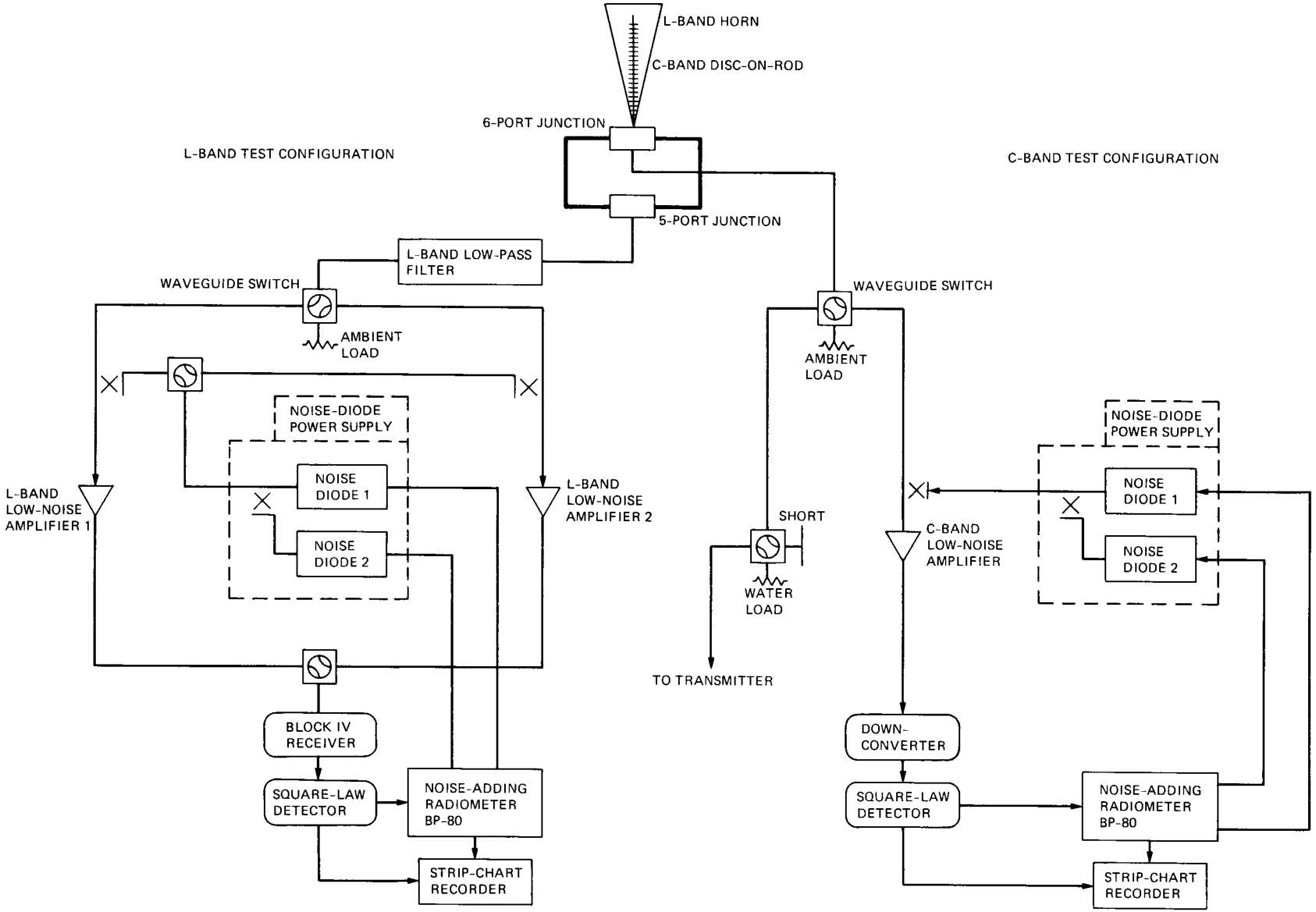


Fig. 1. Block diagram of C/L-band test configuration.

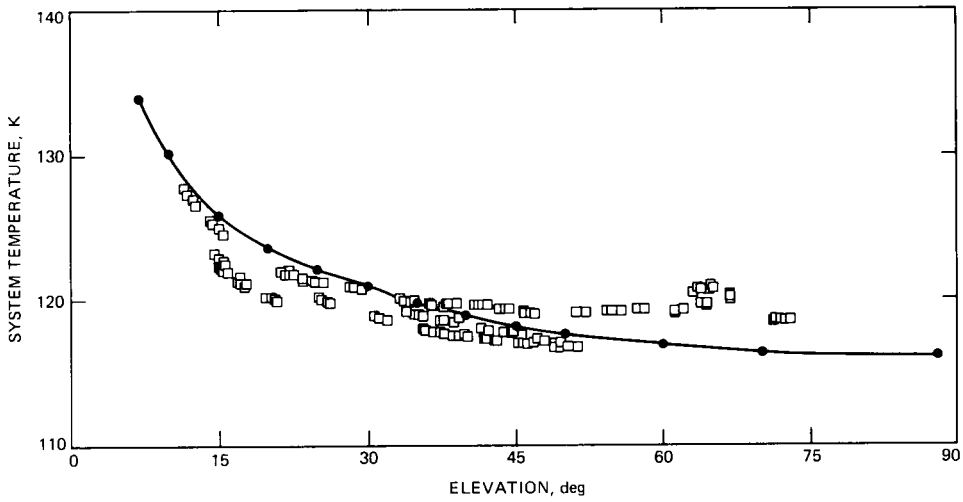


Fig. 2. C-band system temperature.

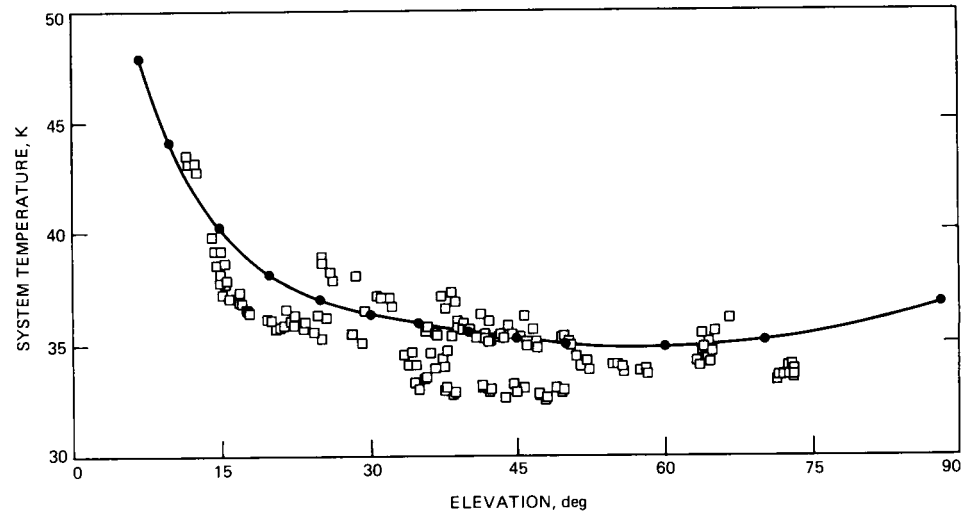


Fig. 3. L-band system temperature.

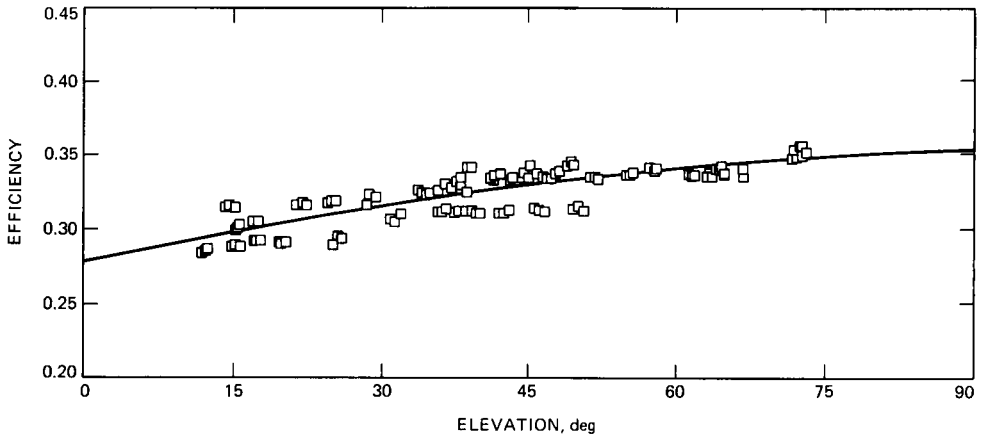


Fig. 4. C-band efficiency versus elevation.

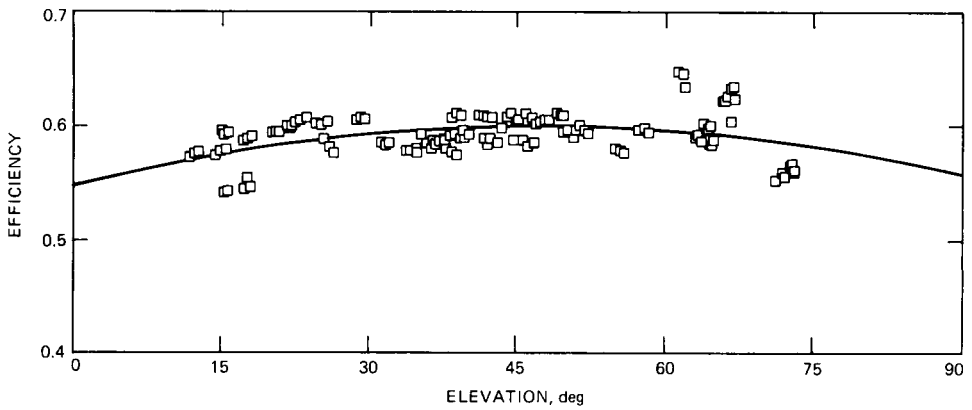


Fig. 5. L-band efficiency versus elevation.

Microwave Time Delays for the Dual L-C-Band Feed System

J. Chen
Ground Antenna and Facilities Engineering Section

A new dual-frequency feed system at Goldstone is designed to receive the Phobos spacecraft signal at L-band (1668 ±40 MHz) and transmit to the spacecraft at C-band (5008.75 ±5.00 MHz) simultaneously. Hence, calculations of the time delay from the C-band range calibration coupler to the phase center of the L-C dual feed and back to the L-band range calibration coupler are required to correct the range measurements. Time delays of the elements in the dual-frequency feed system are obtained mostly from computer calculations and partly from experimental measurements. The method used and results obtained are described in this article.

I. Introduction

The L-C dual-frequency system involves placing a C-band feed inside the L-band feedhorn on the centerline (Fig. 1) [1]. The C-band disc-on-rod, which is physically thin and has minimal effect on the radiation from the L-band feedhorn, was designed using the phase velocity (V_p) data of the disc-on-rod antenna (cigar antenna) [2]. The C-band wave is tightly coupled to the surface of the disc-on-rod so that it is relatively independent of the L-band horn surrounding it. Therefore, the L-band and C-band time delays may be calculated independently.

II. Time Delay at L-Band

The L-band feedhorn and the C-band disc-on-rod compose a coaxial feed which is analyzed using a mode-matching method [3, 4]. In order to apply the coaxial computer program, the disc-on-rod is decomposed into a combination of discs and short rods and the L-band horn is decomposed into short circular waveguides with different radii. There are 585 coaxial sections for the L-C coaxial feed in the program. The program calculates the modes propagating from each discontinuity between coaxial sections from the feedhorn throat to the radiating aperture of the L-band horn. The coaxial program also computes the amplitude and phase of the transmission coefficient (S_{21}) for each mode at each L-band frequency. The three dominant modes are TE_{11}, TM_{11}, and TE_{12}, with power distributions of approximately 81.29 percent, 15.92 percent, and 2.79 percent respectively (Fig. 2). The time delay for each mode is obtained according to the following equation [5]:

$$t_g = \frac{d\phi}{2\pi df}$$

where ϕ is the transmission phase and f is the frequency. The time delay of the L-band is the sum of the time delays of TE_{11}, TM_{11}, and TE_{12} multiplied by the respective power distribution.

The L-band rectangular-to-circular transformer (WR430 to WC504) is designed to have the same cutoff frequency

(1372.24 MHz) in each transformer section. This results in the same group velocity (V_g) in each section.

$$V_g = c\sqrt{1-\left(\frac{\lambda}{\lambda_c}\right)^2}$$

Here c is the speed of light in a vacuum, λ is the wavelength and λ_c is the cutoff wavelength [6]. Hence, for the purpose of calculating group velocity, the transformer may be considered as a piece of straight rectangular waveguide WR430 or circular waveguide WC504. The time delay is equal to L/V_g, where L is the length of the waveguide.

The time delays of the L-band combiner/polarizer and the filter were measured with a Hewlett-Packard 8510 network analyzer. The time delays of all the elements in the L-band system at 1668 MHz are shown in Table 1. The total time delay of the L-band system from the center of the calibration coupler adapter probe to the L-band radiating aperture is 37.935 nsec. This value is then adjusted for the distance to the phase center, which is in the center of the L-band feedhorn and 20 inches away from the L-band feed aperture. The adjusted time delay is 36.443 nsec.

III. Time Delay at C-Band

A C-band corrugated horn (launcher) launches the C-band wave onto the disc-on-rod, which is in the center of the C-band launcher and the L-band feedhorn. Although they also form a coaxial feed, the large radius of the L-band horn with respect to the C-band wavelength makes a complete analysis using the coaxial program impractical. Before entering the L-band feedhorn, the C-band wave is already trapped well onto the disc-on-rod. Since the C-band wave is coupled tightly to the disc-on-rod, it is not influenced by the large-diameter L-band horn. The ratio of free-space wavelength to wavelength on the disc-on-rod antenna as a function of normalized disc depth [1] gives a good estimate of the time delay of the disc-on-rod in free space, which is approximately equivalent to the time delay of the disc-on-rod in the L-band feedhorn. The time delay of the C-band disc-on-rod is calculated partly with the coaxial program and partly using the phase velocity of the disc-on-rod antenna given in [1].

The polarizer (quarter-wave plate) may be considered to be a combination of two coaxial waveguides with different outer radii and a 90-degree phase difference. The time delay of the quarter-wave plate was taken to be the average of time delays of these two coaxial waveguides as computed by the coaxial program.

The rectangular-to-coaxial waveguide junction may be decomposed into the rectangular waveguide and the coaxial waveguide. The time delay of the rectangular-to-coaxial waveguide junction is the sum of the time delay of the rectangular part and the time delay of the coaxial part which was obtained from the coaxial program.

The time delay of each element in the C-band system at 5008.75 MHz is shown in Table 2. The total time delay of the C-band system from the center of the calibration coupler adapter probe to the L-band feed aperture is 25.610 nsec. This value is also adjusted to the phase center of the disc-on-rod which is the same as that of the L-band horn. The adjusted time delay is 23.918 nsec.

Acknowledgments

Special thanks to P. Stanton and H. Reilly for the time delay measurement of the L-band combiner/polarizer and the L-band filter.

References

[1] P. Stanton, "The L-C-Band Feed Design for the DSS-14 70-Meter Antenna (Phobos Mission)," in preparation, Jet Propulsion Laboratory, Pasadena, California.

[2] S. A. Brunstein and R. F. Thomas, "Characteristics of a Cigar Antenna," *JPL Quarterly Technical Review*, vol. 1, no. 2, Jet Propulsion Laboratory, Pasadena, California, pp. 87–95, July 1971.

[3] D. Hoppe, "Modal Analysis Applied to Circular, Rectangular, and Coaxial Waveguides," *TDA Progress Report 42-95*, vol. July–September 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 89–96, November 15, 1988.

[4] R. Hartop, "Microwave Component Time Delays for the 70-Meter Antennas," *TDA Progress Report 42-89*, vol. January–March 1987, Jet Propulsion Laboratory, Pasadena, California, pp. 73–75, May 15, 1987.

[5] G. Mattaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, Sec. 1.05, New York: McGraw-Hill Book Company, 1946.

[6] H. Skilling, *Fundamentals of Electric Waves*, Second Edition, New York: John Wiley & Sons, Inc., 1957.

Table 1. Time delay of each element in the L-band system from the phase center to the center of the calibration coupler adapter at 1668 MHz

Element	t_g, nsec
L-band horn	10.54767
Combiner/polarizer	13.127
Transformer (WR-WC)	1.24856
WR430 (1 in.) × 2	0.14908 × 2
Bent waveguide (7 in. × 7 in. × 90 deg) × 3	1.63918 × 3
Filter (25 in.)	4.6348
Coupler (8.5 in.)	1.26715
Adapter (2.6 in. to center)	0.40251
Total time delay	36.443

Table 2. Time delay of each element in the C-band system from the phase center to the center of the calibration coupler adapter at 5008.75 MHz

Element	t_g, nsec
C-band horn and disc-on-rod	14.27128
Polarizer (quarter-wave plate)	0.80277
Junction (WR-coax)	0.51666
WR187 (44 in.)	4.79729
Bent waveguide (4 in. × 4 in. × 60 deg)	0.68505
WR187 (18.5 in.)	2.01704
Coupler (5 in.)	0.54515
Adapter (2.6 in. to center)	0.28348
Total time delay	23.918

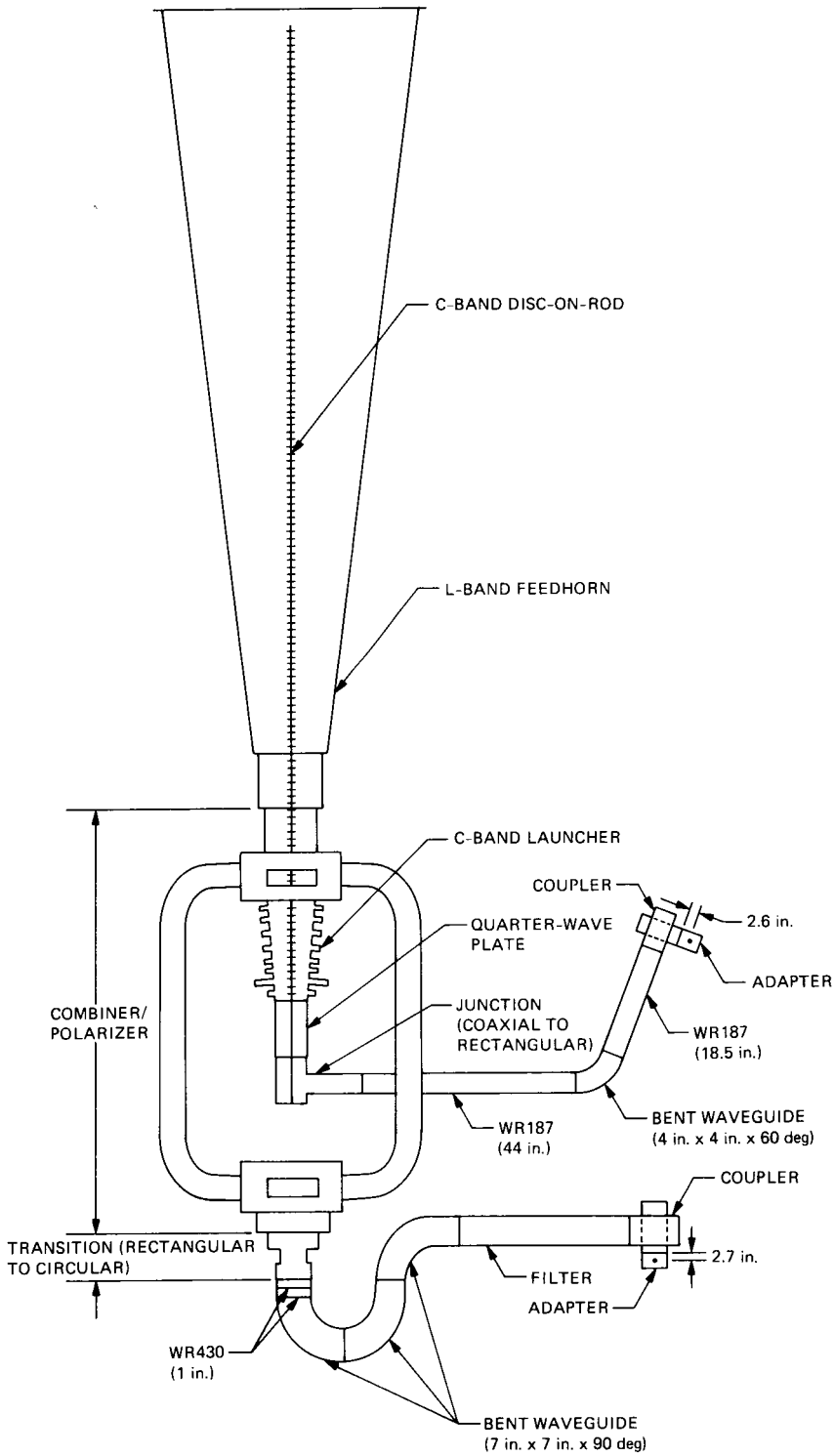


Fig. 1. L-C dual frequency feed system.

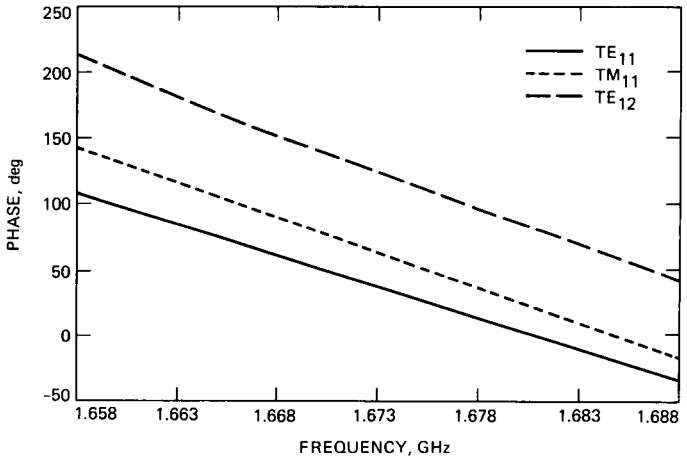


Fig. 2. Phase of the transmission coefficient versus frequency for the L-band feedhorn with a taper.

TDA Progress Report 42-96 October–December 1988

Systems Analysis for DSN Microwave Antenna Holography

D. J. Rochblatt
Radio Frequency and Microwave Subsystems Section

~~This article analyzes~~ proposed systems for Deep Space Network (DSN) microwave antenna holography. Microwave holography, as applied to antennas, is a technique which utilizes the Fourier Transform relation between the complex far-field radiation pattern of an antenna and the complex aperture field distribution to provide a methodology for the analysis and evaluation of antenna performance. Resulting aperture phase and amplitude distribution data are used to precisely characterize various crucial performance parameters, including panel alignment, subreflector position, antenna aperture illumination, directivity at various frequencies, and gravity deformation. Microwave holographic analysis provides diagnostic capacity as well as, perhaps more significantly, a powerful tool for evaluating antenna design specifications and their corresponding theoretical models. Functional requirements, performance, and potential for future technological growth are considered, leading to a description of complete in-house DSN capability for operational "health checks," evaluations, diagnostics, and performance optimization, as well as a flexible R&D tool for further development of large antennas. Wide-bandwidth, narrow-bandwidth, and phase-retrieval systems are analyzed and discussed with respect to three relevant signal sources: a natural radio star, a satellite channel of perhaps telephone or computer data that can be treated as a Gaussian noise source, and a satellite CW beacon. A recommendation based on systems analysis is made to first implement the narrow-bandwidth CW system. It will provide high-resolution and low-resolution holographic maps with high precision suitable for individual panel setting, and function as a flexible R&D engineering tool offering future growth potential. With modest software addition, a wide-bandwidth 1-bit correlator could become part of that system, providing low-resolution maps in the DSN frequency bands that satisfy the requirement for a quick response to operational needs. Since the implementation of 1-bit correlators in the DSN stations is not envisioned before 1994, and since DSN Operations desires a low-cost implementation of quick "health check" diagnostic capabilities as soon as possible, it is recommended that a phase-retrieval-based holography system be developed for that purpose.

I. Introduction

Microwave antenna holography implementation for the DSN must satisfy at least three primary requirements. First, it must satisfy DSN Operations' need for a quick "health check" of the antenna mechanical and microwave subsystems to yield an unambiguous go/no go operational antenna status result. The holography measurement must be conducted within the DSN frequency bands using the operational microwave front-end equipment. To derive the required quantitative parameters, holographic maps of low resolution and medium accuracy are sufficient. The measurement time needed for these maps is

about 30 minutes, and will be conducted by antenna operators using transferred hardware and software.

Second, the system must satisfy DSN Operations' implementation needs for accurate reflector panel setting adjustments. To derive the required quantitative parameters, holographic maps of high resolution and high precision are needed. To complete the data acquisition measurement for these maps, 12 hours are needed for the 70-m antennas and 6 hours for the 34-m antennas. It is recommended that the holography system chosen promise future reduction in measurement time as stronger signal sources become available. This panel setting mode is not expected to be used frequently. Therefore, a special test equipment mode of operation by a station engineer/analyst could be used. The data processing and detailed diagnostics of the data need not be the responsibility of station personnel and might be done at JPL.

Third, a DSN microwave holography system must provide future technological growth potential in terms of measurement precision, data acquisition speed, and in understanding the performance limitations of large, efficient microwave reflector antennas for deep space communications. Microwave holography will provide a major tool in future studies of understanding a broad range of factors that affect antenna performance, including: reflector panel manufacturing; setting precision; beam pointing; focus; gain; phase stabilities; mechanical hysteresis; and weather, paint, aging, thermal, and wind effects.

The measurement system selected must support the DSN's need to acquire every 0.1-dB gain improvement available from its major antennas, and must also support the operational need for a quick "health check," including first-order evaluations of the mechanical antenna and microwave front end.

The operational measurement system must be compatible with the antenna operational configuration. Both conventional and beam waveguide 32-GHz antennas must be supported. The use of non-DSN frequencies, feeds, or amplifiers/receivers should be minimized or eliminated if possible. Commercial equipment that includes manufacturer support for a 10-year period must be carefully selected.

II. Requirements Summary

The parameters critical for the quality of the images derived from holographic measurements are signal-to-noise ratio (SNR), instrumentation dynamic range, and overall measurement system accuracy. A detailed mathematical derivation of the related equations can be found in [1–3].

In the first "health check" mode of operation, a lateral resolution of typically D/20 is necessary, which can be achieved with a data array size of 25 X 25. The standard deviation of the image error profile need be no better than $\lambda/100$, and optimum subreflector settings need be no better than $\lambda/10$ at 8 GHz. When the antenna scan rate traverses a sidelobe per second and allows sample smearing of 5 to 10 percent, an integration time of 0.1 sec is indicated. Under the above conditions, it will take 30 minutes to produce a 25 X 25 array. To achieve image quality with a standard deviation of 0.5 mm on the 70-m or 34-m antennas with lateral resolutions of D/20, an approximate beam-peak SNR of 45 dB (in an integration period of 0.1 sec) is required at X-band (8.4 GHz), or 42 dB at Ku-band (11.45 GHz). (To achieve the same specifications with phase-retrieval holography, as described in Section IV, an approximate beam-peak SNR of 60 dB is required at S-band [2.2 GHz].)

In the second panel-setting mode, the large number of individual panels (each with an area of 2 m^2) on the 70-m and 34-m antennas (arranged in 17 and 9 circumferential rings, respectively) dictates a high lateral resolution of about 0.35 m. Array data sizes of 197 X 197 and 127 X 127 for the 70-m and 34-m antennas, respectively, are necessary. The two-dimensional far-field pattern must be sampled out to approximately the 90th (60th) sidelobe for the 70-m (34-m) antenna to provide the required resolution. Since the antenna far-field radiation pattern falls off rapidly away from beam peak, a specification of system dynamic range greater than 80 dB is necessary for measurement to the 90th sidelobe. For a maximum of 0.1-dB degradation in antenna efficiency due to random surface imperfections, the rms surface error must be no greater than 0.012λ. This translates to an rms surface error of 0.43 mm at X-band (8.4 GHz) and 0.11 mm at Ka-band (32 GHz). To achieve surface error maps with one standard deviation of 0.1 mm at resolution cell size of 0.35 m for the 70-m antenna, a beam-peak SNR of 73 dB is required at Ku-band (11.45 GHz) and 75 dB at X-band (8.4 GHz). On the average, there are 25 data points on each panel, which provide screw adjustment accuracy of 0.02 mm. Theoretically, one calculates that an 87-dB SNR would be required at S-band (2.2 GHz). However, diffraction effects at this frequency contaminate the holographic images, making the data unsuitable for precise panel setting. To achieve the same accuracy on the 34-m antenna, a beam-peak SNR of 66 dB is required at Ku-band and 69 dB at X-band [3]. The accuracy of the subreflector position correction will typically be 0.5 mm.

The accuracy across holographic maps varies with the aperture amplitude taper illumination. Results are better at the center of the dish and gradually become worse toward the edge of the dish. For a uniformly illuminated dish, accuracy stays relatively constant through most of the dish and becomes quickly worse just at the edge where the illumination falls off

rapidly. The values calculated here are at the position of average amplitude taper value.

Antenna scan rates, signal SNR, signal source orbit stability, integration time, and sample smearing constraints lead to a 12-hour (presently nighttime) measurement time for the 70-m antenna (6 hours for the 34-m antenna) to obtain the high-resolution high-precision maps. A decrease in measurement time is desirable and can only be achieved with a receiver system compatible with the signal source. Such a system will provide higher SNR at shorter integration time periods as stronger signal sources become available. The narrow-bandwidth system matched to satellite CW signals can provide this future capability. This will allow low-resolution (25 X 25) image data acquisition in approximately 15 minutes. Meaningful wind and thermal information, for example, would become available for the first time with such fast imaging capture. Additional system requirements include antenna pointing precision of ±0.002 deg and angle encoder sampling intervals of 10 msec.

III. Systems Analysis

A. Wide-Bandwidth System

For the implementation of the 1-bit A/D and the 1-bit correlator for holographic measurements, three cases must be considered, as in each, the 1-bit correlator operates differently:

Case I: Weak signal—either a CW or Gaussian noise source

Case II: Strong CW signal

Case III: Strong Gaussian noise source

For two antennas with system temperatures T_{s1} and T_{s2}, which are pointed at a source giving antenna temperatures T_{a1} and T_{a2}, with channel bandwidth B (Hz) and an integration period of T (sec), the SNR of the correlated fringe amplitude to rms noise is

$$SNR = \eta \sqrt{\left[\frac{T_{a1}\, T_{a2}}{(T_{s1} + T_{a1})(T_{s2} + T_{a2})}\right][2BT]} \qquad (1)$$

where η is a factor accounting for losses due to quantization and processing. The loss factors are multiplicative, so the total loss is given by

$$\eta = \eta_Q\, \eta_R\, \eta_S\, \eta_D \qquad (2)$$

where

η_Q = quantization loss for 1 bit, two-level is $2/\pi$ (0.637)

η_R = fringe rotation loss for three-level, one path is 0.960

η_S = loss due to fringe counter rotation, one channel is 0.707 ($1/\sqrt{2}$)

η_D = discrete delay step loss, which for spectral correction is 1.00

Conservatively, $\eta = 0.432$ (–7.3 dB).

For Case I, $T_{ai} \ll T_{si}$, and the SNR (Eq. 1) can be reduced to

$$SNR_I = 0.43 \sqrt{\left[\frac{T_{a1}\, T_{a2}}{T_{s1}\, T_{s2}}\right][2BT]} \qquad (3)$$

For Cases II and III, $T_{ai} \gg T_{si}$, and the SNR equation becomes

$$SNR_{II,III} = 0.43\sqrt{2BT} \qquad (4)$$

and is independent of the size of the antennas because the SNR is determined by the fluctuations in signal level. That is the saturated condition [4].

Only when a 1-bit correlator is operating under Case I conditions (Eq. 3) can it provide accurate amplitude and phase measurements. When the correlator is operating under Case II or III, it can no longer provide amplitude measurements, as the correlation (ρ) is equal to a constant equal to 1:

$$\rho_{T_{ai} \gg T_{si}} = \sqrt{\frac{T_{a1}\, T_{a2}}{(T_{s1} + T_{a1})(T_{a2} + T_{s2})}} = 1 \qquad (5)$$

However, it can still provide accurate phase measurement if the observable is a Gaussian noise source. If the observable is a CW signal, neither accurate phase nor amplitude measurement can be obtained (assuming Nyquist sampling rate)[1] [5, 6]. It can be shown[2] that for a sinusoidal signal $y(t)$ buried in Gaussian noise $n(t)$ which has a normalized probability density function

$$G(x) = \frac{1}{\sqrt{2\pi}} \exp\left[\frac{-x^2}{2}\right] \qquad (6)$$

[1] E. H. Sigman, "Phase Measurement of Sinusoidal Tones Buried in Noise," JPL Engineering Memorandum 315-74 (internal document), November 1978.

[2] Ibid.

with standard deviation $\sigma = 1$, the detected signal at a particular time t_1 at the output of a 1-bit A/D converter is

$$d(t_1) = \frac{2N}{\sqrt{2\pi}}\left[y_1 - \frac{y_1^3}{6} + \frac{y_1^5}{40} - \cdots\right] \tag{7}$$

where $y_1 = y(t_1)$ and N is the number of samples. To allow the higher-order terms to contribute less than 1 deg of phase noise error, the condition

$$y_1 \leqslant 0.32$$

must be met, and to allow a maximum amplitude error of ±0.3 dB, the condition

$$y_1 \leqslant 0.64$$

must be met. This constrains the upper-limit SNR (and dynamic range) for sensibly linear operation of the 1-bit correlator.

For simplicity, one may summarize that for accurate amplitude measurements with the 1-bit correlator using CW or Gaussian noise sources, the condition

$$T_{ai} \leqslant 0.5\, T_{si}$$

must be met. In the CW case, this is also the upper-limit condition for accurate phase measurements. (In principle, oversampling could solve this problem. However, since the CW signal is not compatible with the 1-bit correlator architecture, this application is not elaborated upon.)

The best possible performance available from a 1-bit digital correlator can now be analyzed.

1. Case I. One of the strongest usable natural radio sources at X-band is 3C84, with a flux density of 46.6 Jy.[3] For a short baseline, such as between a 70-m and 34-m antenna at the same complex, it is unresolved.

Assuming 65 percent efficiency for both 70-m and 34-m antennas, $T_{a1} = 42.21$ K for the 70-m antenna and $T_{a2} = 9.95$ K for the 34-m antenna with $T_{s1} = T_{s2} = 30$ K. T_{a1} does not satisfy the linearity condition, but since it is only about 4.6 dB away, one may ignore it for a moment, assuming a simple solution can be provided. The MKIIIA 1-bit real-time correlator, designed at the Haystack Observatory, has a channel bandwidth of 2 MHz, and JPL is planning to integrate 10 channels in July 1989.

[3] Jy = 10^{-26} W/m^2 Hz.

Assuming an integration time of 0.1 sec and 1 channel, the beam-peak SNR can be calculated using Eq. (3):

$$SNR_{max} = 0.43\sqrt{\left[\frac{(42.21)(9.95)}{(72.21)(39.95)}\right][(4)(10^6)(0.1)]}$$

$$= 103.77$$

This is an SNR of 40.3 dB.

To calculate the dynamic range, take $SNR = 1$ as a reference minimum, then

$$SNR_{min} = 1$$

$$= 0.43\sqrt{\left[\frac{(T_{a1_{min}})(9.95)}{(72.21)(39.95)}\right][(2)(2)(10^6)(0.1)]} \tag{8}$$

$$T_{a1_{min}} = 0.0039 \text{ K}$$

and the dynamic range

$$DR = \frac{T_{a1_{max}}}{T_{a1_{min}}} = \frac{42.21}{0.0039} = 10823 \text{ or } 40.3 \text{ dB}$$

Assuming all ten channels[4] can be utilized in a real-time measurement configuration

$$SNR_{max} = 51 \text{ dB}$$

It has already been shown [3] that a Move-Stop-Integrate approach to DSN holography is totally unacceptable. However, assuming that the antenna can be moved slowly enough (as long as it is stable) to relax the integration time requirements to perhaps 0.5 sec (only acceptable for low-resolution scans),

$$SNR_{max} = 58 \text{ dB}$$

[4] In the current operational architecture of the Haystack correlator and its interfacing computer, the minimum integration period that can be achieved with multi-channels is 0.5 sec. No changes to the Haystack design are planned at JPL. The above analysis assumes a new computer design, and interfaces to the correlator to achieve the required 0.1-sec integration period capability would be provided (private communication, Charles Edwards).

It is anticipated that for the year 1992, a 1-bit correlator with a bandwidth of 16 MHz will be operational at JPL.[5] With this in place, a 50-dB SNR_{max} could be obtained with a 0.1-sec integration period.

2. Case I: Summary. As can be seen, the integration period and the bandwidth in the correlator are the critical parameters for obtaining high SNR and dynamic range, and are the limiting factors (assuming all the bandwidth needed is available from the radio star). Using a 1-bit correlator to obtain low-resolution holographic images is feasible and valuable for the DSN in-band holographic quick "health check" measurements. An estimated array size of up to 51 X 51 providing lateral resolution of approximately 1.6 m (0.8 m) with accuracy of 0.2 mm can be delivered for the 70-m (34-m) antenna. The source would be tracked near meridian transit to minimize elevation angle changes. Two large DSN antennas would have to be allocated for the measurement.

3. Cases II and III: Strong Source Case. The most effective strong sources are obtained from geostationary satellite downlink channels. Only the portion of the channel bandwidth that is continuously occupied is useful for the correlator. In addition, wide-bandwidth signals are more favorable than narrow-bandwidth signals (even if the narrowband signal is of stronger EIRP) in terms of SNR and dynamic range in the 1-bit correlator system, since saturation and non-linearity occur if T_a exceeds the level specified above. For now, the CW case shall be ignored and instead the alternative wideband downlink signals will be considered. Some communication satellite telephone and data links have the characteristics of Gaussian random noise. In terms of the correlator performance, they can be treated as extremely strong natural radio point sources of limited bandwidth.

About one quarter of all communication satellites have wide-bandwidth data-link signal characteristics that are useful for holographic measurements. Data links that do not occupy the channel bandwidth continuously are of no use, and those that fluctuate in intensity are serious sources of error in the correlator measurement system. Since the correlator multiplies the two channels, any amplitude variation in the signal level will not be canceled, and will cause an error in the holographic maps. This characteristic alone is considered a major drawback. Unlike the natural radio sources of large bandwidth, the satellite channel bandwidth is limited, and most of the time only a portion of the spectrum has adequate characteristics; 0.5 MHz is conservatively chosen.[6] Theoretically, one could rent a transponder on a satellite, thereby enabling an adequate wide-bandwidth noise source. This approach is considered to be impractical. Typically, the satellite signals will produce a T_a on both test and reference antennas greater than 40 dB (70-m antenna) and 34 dB (34-m antenna) above T_s.

For example, assume that when the test antenna (70-m) is observing the signal on beam peak, $T_a(\text{dB}) - T_s(\text{dB}) = 40$ dB, which is a practical consideration. Under this condition, only when the test antenna scans −43 dB below the beam peak (as shown earlier), does the correlator enter into its linear region. Taking a 0.1-sec integration period:

$$SNR_{max} = (0.43)(0.33)\sqrt{(2)(0.5)(10^6)(0.1)}$$

$$SNR_{max} = 33 \text{ dB}$$

assuming a Ku-band measurement and $T_{si} = 200$ K.

From the simple analysis above, it is seen that for strong satellite signal sources, when $T_a \gg T_s$ (hence, the reference antenna channel is saturated), the SNR and dynamic range of the 1-bit correlator are functions of the bandwidth (which is limited by the satellite) and the integration time. Since the SNR is independent of the size of the antennas, a small reference antenna should be used (D ~ 2 m) for economy. One way of overcoming the limited dynamic range of the correlator is to use a radiometer in conjunction with the correlator. Under this split architecture, the radiometer is used to measure amplitudes at signal levels above which the correlator is saturated, and the correlator provides phase information. As the antenna measurement proceeds down to its sidelobes, the radiometer is reaching its noise floor, and the correlator enters into its linear region, providing amplitude and phase measurement capability (Fig. 1).

4. Cases II and III: Summary. Even with strong satellite signal sources, the 1-bit correlator by itself has a limited dynamic range for its linear region as a phase/amplitude measurement system. The limited satellite bandwidth and short integration period required limit the correlator's linear dynamic range to about 33 dB (which is less than what can be achieved with radio stars of wide bandwidth, i.e., 50 dB).

With Gaussian noise-like signals, the correlator can provide accurate phase measurement, even in its non-linear region, and with the addition of another instrument (e.g., a radiometer), an overall large dynamic range can be achieved equal to the sum of the correlator dynamic range plus ($T_{a_{max}}$(dB) − T_s (dB)). Unavoidable signal level fluctuations and the fact that the correlator is a channel multiplication device could produce serious sources of error in the holographic map than cannot be

[5] Dave Rogstad, private communication.

[6] B. Corey (Haystack Observatory) and W. Johnson (Multicomm, Inc., Arlington, Virginia), private communication.

recovered without additional instrumentation. Using two separate instruments to measure a complex quantity, one device measuring amplitude while the other provides phase, is an undesirable approach. Using two separate instruments in an overlapping fashion (as one saturates on its upper SNR the other reaches its lower limit) is clearly not a recommended instrumentation approach. There are other feasible ways to extend the dynamic range of the 1-bit correlator. For example, switched attenuators may be incorporated to drive the correlator into its linear range at strong signal levels. The attenuators can then be switched out at the lower signal level, maintaining the correlator in its linear range. None of these techniques, however, can take advantage of stronger satellite signal sources and provide a larger SNR at the correlator output. All they do is extend the dynamic range of the 1-bit correlator. This is the result of a fundamental mismatch between strong signals and the 1-bit correlator architecture. In view of the above, and since better system solutions are available, additional analysis for Cases II and III is unnecessary.

Some radio astronomy observatories perform limited holographic measurements using the above approach because of the availability of the instruments already connected to their system. (See summary in Table 1.)

B. Narrow-Bandwidth System

The narrow-bandwidth system can be designed with a wide dynamic range and linear response. A narrow-bandwidth receiver/data acquisition system design and recommendation for JPL holography implementation was formally proposed in October 1985.[7] The system makes use of geostationary satellite beacon signals (nearly CW) available on nearly all satellites at Ku-band (11.45 GHz), X-band (7.7 GHz), S-band (2.2 GHz) and perhaps on other bands in the future. The IF section of the new HP 8510B network analyzer phase locked with an HP 8530B sweep oscillator could provide the heart of this system architecture (Fig. 2). Rather than cross-correlating the two channels, which is a multiplicative operation, the HP 8510B uses synchronous detectors for the I and Q components of the test and reference channels. After digitization (19-bit resolution A/D converter), the ratio of test-to-reference channel is formed to provide the real and imaginary components of the complex far-field function. Amplitude variations in the satellite signal cancel out in the division operation. This feature is especially critical since no control over the satellite signal power level is reasonable. Also, since the reference channel SNR in this scheme can easily be 40 dB or better, it can be safely used in the denominator (this would not be desirable for weak reference signals). Doppler frequency changes and phase jitters due to satellite signal instabilities will produce a frequency difference between the second local oscillator (LO) and IF signals (Fig. 2) that will be measured by the HP 8510B, which then generates an error signal that phase locks the LO to produce the 20-MHz second IF input to the HP 8510B.

The HP 8510B provides a linear dynamic range of better than 96 dB down to integration periods of 0.2 msec (which covers the future high-resolution, high-speed 70-m/4-hr goal). With a satellite beacon EIRP of about 11 dBW, a beam-peak SNR of 73 dB can be achieved on the 70-m antenna with a 0.1-sec integration period and a simple room-temperature FET amplifier, while a 2.8-m reference dish can provide more than 44 dB in SNR using a room-temperature FET.

For the HP 8510B architecture, it can be shown that the effective signal SNR is

$$SNR_E = \frac{1}{\sqrt{\frac{1}{SNR_T^2} + \frac{1}{SNR_R^2} + \frac{1}{SNR_T^2\, SNR_R^2}}} \tag{9}$$

where SNR_T and SNR_R are the test channel SNR and reference channel SNR, respectively. This expression is also correct for a multiplier integrator as well as a divider integrator.

From Eq. (9), it is apparent that the effective SNR_E is dominated by the weaker of the two channels. What this means is that the beam-peak SNR of 73 dB is not realized, and the first few data points on beam peak and a few sidelobes have an effective SNR of 44 dB (the reference SNR). Once the test channel SNR drops below 44 dB, the reference antenna does not hurt the effective SNR_E, which, from that point, follows the same function as the test antenna beam patterns (SNR_T). Also, since very few data points are affected (approximately 0.5 percent), and since by the nature of the data processing through the Fourier Transform operation all the data points in the far-field contribute to each and every point in the aperture, this is acceptable, as shown below.

To evaluate the suitability of the HP 8510B architecture with a small reference antenna, a simulation algorithm was written in which each channel of the I and Q components of both the test and reference channels had added independent noise processing components n, for which the one sigma (1σ) in the random Gaussian function are

$$1\sigma_T = \frac{Amp_T(\theta_{max})}{SNR_T(\theta_{max})} \tag{10}$$

[7] D. J. Rochblatt, "JPL Holography Review" (internal document), October 10, 1985.

and

$$1\sigma_R = \frac{Amp_R}{SNR_R} \tag{11}$$

for the test and reference signals, respectively. The function of the IF section of the HP 8510B was simulated to provide the resultant measured complex quantity including noise:

$$\text{Measured Complex Field} = \frac{Amp_T(\theta_i)\, e^{j\phi_{Ti}} + n_{R_i}^T + jn_{I_i}^T}{Amp_R\, e^{j0} + n_{R_i}^R + jn_{I_i}^R} \tag{12}$$

where the real and imaginary components of the noise processing are denoted by subscripts R_i and I_i, respectively. During this simulation, the effect of the SNR of the reference and test antennas on measurement accuracy was examined.

In the simulation, four rings of panels were intentionally displaced by 0.2 mm (λ/130 at 11.45 GHz). Three rings were displaced positively and one was displaced negatively. The width of the three outermost rings is 2.0 m (76λ) and the innermost ring is 1.0 m wide. The rms surface error of this model is 0.11 mm. The far field for the above reflector geometry was generated [7] and then contaminated with noise, due to the front end, according to the Eq. (12) model. The far-field data were then processed by the JPL DSN holography software [8] to display the recovered surface error maps and compute the surface rms errors.

In Simulation I (Figs. 3 and 4), the far field was processed with no noise added to it. This simulated an SNR of more than 90 dB. The computer computational errors are at a level of about λ/5000 (11.45 GHz). By subtracting the Simulation I model from subsequent simulations (map differencing), a measure comparable to measurement system standard deviation is obtained.

Simulation II (Figs. 5, 6, and 7; note the different scales in the cut plot between Simulation I and all subsequent simulations), models the conditions where the test antenna SNR on beam peak in a 0.1-sec integration period is 78 dB and the reference antenna constant SNR is 40 dB. These conditions are stated as a goal but are not usually achieved in practice. The recovered rms of the test antenna surface is 0.11 mm and the measurement system standard deviation is 0.04 mm (λ/650 at 11.45 GHz).

Simulation III (Figs. 8, 9, and 10) simulates the presently achievable condition in which the test antenna beam peak SNR in a 0.1-sec integration period is 73 dB and the reference antenna SNR is 40 dB. The recovered surface rms is 0.12 mm with a standard deviation of 0.07 mm (λ/370 at 11.45 GHz). In the cut plot, Fig. 9 in this case, the aperture amplitude taper of −13 dB was superimposed for demonstration of increased error in the image toward the edge of the dish. Simulations IV, V, and VI (Figs. 11 through 19) and Table 2 demonstrate the conditions of decreasing SNR in the test channel and increasing SNR in the reference channel in 5-dB steps. The necessity of high beam-peak SNR for high-resolution, high-precision holographic measurement is clearly demonstrated. Also, the limited contribution of reference channel SNR in compensation for low test-channel SNR is demonstrated and shown. The limited contribution of the reference channel SNR-to-surface error reconstruction relates to the relatively small number of data points being affected (0.5 percent for the case 73 dB/40 dB), and to the physics, i.e., the small surface distortions (high frequency) affect mostly the sidelobes farther away from the beam peak [3]. Thus, one of the more important functions of the reference SNR in the CW case is to keep the receiver in phase lock with the carrier.

IV. Phase Retrieval Holography

The phase retrieval holography retrieves phase information from a measurement of the antenna far-field intensity only. Since phase is not directly measured, a second reference antenna and a two-channel receiver or correlator are not necessary. The in-place receiver and front end are used to measure the antenna far-field intensity function. For more details about the technique, see Appendices A and B.

Because of the limitations of this technique, it is only recommended for low-resolution holographic imaging sufficient for operation and maintenance quick "health check" needs. For such application, it is estimated that a beam-peak SNR of 60 dB is required in order to achieve the same precision over a 25 X 25 size array as would be achieved with true holographic (amplitude and phase) measurements. If radio star sources and a radiometer measurement system are used, a square root reduction in SNR is suffered (due to incoherent processing) relative to coherent processing using a two-channel correlator. Satellite CW beacon signals are available at S-band (2.2 GHz) from DSCS satellites, viewable at all DSN complexes with high achievable SNR and are therefore recommended for this approach.

V. Summary and Conclusion

Based on the far-field signal sources available, a narrow-bandwidth measurement system is superior in performance to a broad-bandwidth system based on a 1-bit real time correla-

tor (20-MHz BW) for high-resolution/high-precision panel setting holography. A multi-bit correlator is a better candidate for holographic measurement[8] because it provides wider dynamic ranges. In the cases where the correlator is of multi-bits, or when a synthesis signal is correlated against the 1-bit correlator, phase locking becomes necessary and essentially one comes back to an HP 8510B type of architecture.

The 1-bit correlator (Haystack, MKIIIA), expected at JPL in about one year (although implementation at all DSN complexes is not envisioned before 1994), would be useful for low-resolution holographic measurement in the DSN frequency band using natural radio sources. It has the advantage that no feeding/receiver changes need to be made for the measurement, allowing quick response to a demand for an antenna "health check." However, a second large antenna (34-m or 70-m) would have to be allocated for such measurements.

Phase retrieval holography is especially attractive for quick "health check" antenna diagnostics. Only one antenna (the antenna under test) is used, utilizing existing station receivers and front end within S-band. It is a minimal cost solution that could prove powerful for low-resolution holography.

[8] D. J. Rochblatt, "Digital-Multibit-Correlator/Remarks," JPL IOM 3331-84-053 (internal document), July 20, 1984.

For high-resolution, high-precision panel setting holography and future growth potential, the narrow-bandwidth/CW system provides significant advantages, and hence it is recommended here. In addition, this system will also perform low-resolution "health check" measurements in a shorter time with higher precision (see Table 1), albeit not in the DSN frequency bands. With some design modifications, the DSN advanced receiver could be utilized to advantage in the future.

Most of the software (80 percent) that is required for data acquisition and correction is independent of the hardware (it will apply for the narrow-bandwidth as well as the 1-bit correlator system). Also, all the JPL DSN holography data processing and the holography software methodology developed in-house thus far are independent of the system hardware.

It is strongly recommended that the DSN initiate holography capability with a narrow-bandwidth system capable of both high- and low-resolution holography measurements. An HP 8510B or other commercial instrument (with manufacturer's support for perhaps 10 years) is recommended as the heart of the narrow-bandwidth high/low-resolution implementation. With modest software addition, the wide-bandwidth 1-bit correlator could become part of that system, providing low-resolution maps in the DSN frequency band. Phase retrieval holography is especially attractive for satisfying the requirement for a quick response to DSN Operations' needs.

Acknowledgments

The author wishes to thank Brooks Thomas of the Tracking Systems and Applications Section for his many helpful technical discussions and contributions. In addition, thanks are due to D. Bathker and B. Seidel for brainstorming discussions, and to V. Galindo for his contributions to the minimization technique described in Appendix B.

References

[1] P. F. Scott and M. Ryle, "A Rapid Method for Measuring the Figure of a Radio Telescope Reflector," *Mon. Not. Roy. Astr. Soc.*, vol. 178, pp. 539–545, 1977.

[2] L. R. D'Addario, "Holographic Antenna Measurements," *Memo No. 202*, National Radio Astronomy Observatory, Charlottesville, Virginia, pp. 1–20, November 1982.

[3] D. J. Rochblatt and B. L. Seidel, "DSN Microwave Antenna Holography," *TDA Progress Report 42-76*, vol. October–December 1983, Jet Propulsion Laboratory, Pasadena, California, pp. 27–42, February 15, 1984.

[4] A. R. Thompson, J. M. Moran, and G. W. Swenson, Jr., *Interferometry and Synthesis in Radio Astronomy*, New York: John Wiley & Sons, Inc., pp. 155–168, pp. 247–305, 1986.

[5] J. H. Vleck and D. Middleton, "The Spectrum of Clipped Noise," *Proceedings of the IEEE*, vol. 54, no. 1, pp. 1–56, January 1966.

[6] J. B. Thomas, "An Analysis of Long Baseline Radio Interferometry, Part II," *JPL Technical Report 32-1526*, vol. VIII, 1972.

[7] Y. Rahmat-Samii and D. J. Rochblatt, "Effect of Measurement Errors on Reflector Surface Reconstruction Using Microwave Holographic Metrology," *Proceedings of the Antenna Measurement Techniques Association*, Seattle, Washington, pp. 174–179, Sept. 1987.

[8] D. J. Rochblatt, Y. Rahmat-Samii, and J. H. Mumford, "DSN Microwave Antenna Holography Part II: Data Processing and Display of High Resolution Effective Maps," *TDA Progress Report 42-87*, vol. July–September 1986, Jet Propulsion Laboratory, Pasadena, California, pp. 92–97, 1986.

[9] R. E. Burge, "The Phase Problem," *Proc. R. Soc. Lond. A.*, vol. 350, pp. 191–212, 1976.

[10] A Walter, "The Question of Phase Retrieval in Optics," *Opt. Acta*, vol. 10, pp. 41–49, 1963.

[11] R. W. Gerchberg and W. O. Saxton, "A Practical Algorithm for the Determination of Phase from Image and Diffraction Plane Pictures," *Optik*, vol. 35, pp. 237–246, 1972.

[12] D. L. Misell, "A Method for the Solution of the Phase Problem in Electron Microscopy," *J. Phys. D., Appl. Phys.*, vol. 6, pp. L-6–L-9, 1973.

Table 1. System performance (70-m antenna)

System type	Bandwidth, MHz	Signal source	Frequency, GHz	D_R, m	T, sec	SNR_{max}, dB	DR, dB	Array size, n × n	δ, m	σ, mm	Measurement time, hr
A	2	3C84	8.4	34	0.1	40.3	40.3	25 × 25	3.3	0.80	0.5
A	20	3C84	8.4	34	0.1	51	51	25 × 25	3.3	0.24	0.5
A	20	3C84	8.4	34	0.5	58	58	51 × 51	1.6	0.22	4.0
A[a]	0.5	Satellite	11.45	34/2.8	0.1	33	73	127 × 127	0.65	0.3	6.0
B	0.01	Satellite Beacon	11.45	2.8	0.1	73	96	197 × 197	0.40	0.1	12.0
B[b]	0.01	Satellite Beacon	11.45	2.8	0.02	73	96	197 × 197	0.40	0.1	4.0
B	0.01	Satellite Beacon	11.45	2.8	0.1	73	96	127 × 127	0.65	0.06	6.0
B	0.01	Satellite Beacon	11.45	2.8	0.1	73	96	25 × 25	3.3	0.012	0.5
B[b]	0.01	Satellite Beacon	11.45	2.8	0.02	73	96	25 × 25	3.3	0.012	0.25
C	TBD	Satellite Beacon	2.2	Not Needed	0.1	73	73	32 × 32	3.3	0.2	0.25

A = Wide-bandwidth system
B = Narrow-bandwidth system
C = Phase retrieval
D_R = Reference antenna diameter
T = Integration period
DR = Dynamic range
δ = Lateral resolution
σ = Standard deviation of surface profiles

[a]With added radiometer for amplitude measurements and assuming $T_{a_{max}}/T_s = 4$ dB.

[b]Possible future capability.

Table 2. Narrow-bandwidth system simulations (64-m/2.8-m antennas)

Simulation No.	$SNR_{T_{max}}$, dB	SNR_R, dB	Recovered surface rms, mm	Measurement system standard deviation, mm	Figures
I	>90	n/a	0.11	0.005	3, 4
II	78	40	0.11	0.04	5, 6, 7
III	73	40	0.12	0.07	8, 9, 10
IV	68	45	0.16	0.13	11, 12, 13
V	63	50	0.25	0.23	14, 15, 16
VI	58	55	0.43	0.41	17, 18, 19

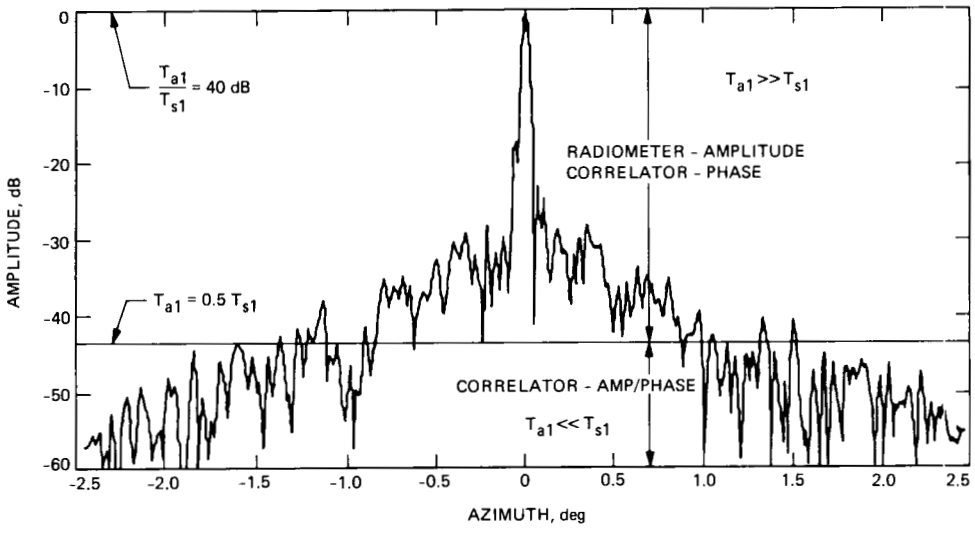


Fig. 1. Conceptual measurement scheme utilizing broadband satellite channels and radiometer/correlator in an overlapping, saturation mode.

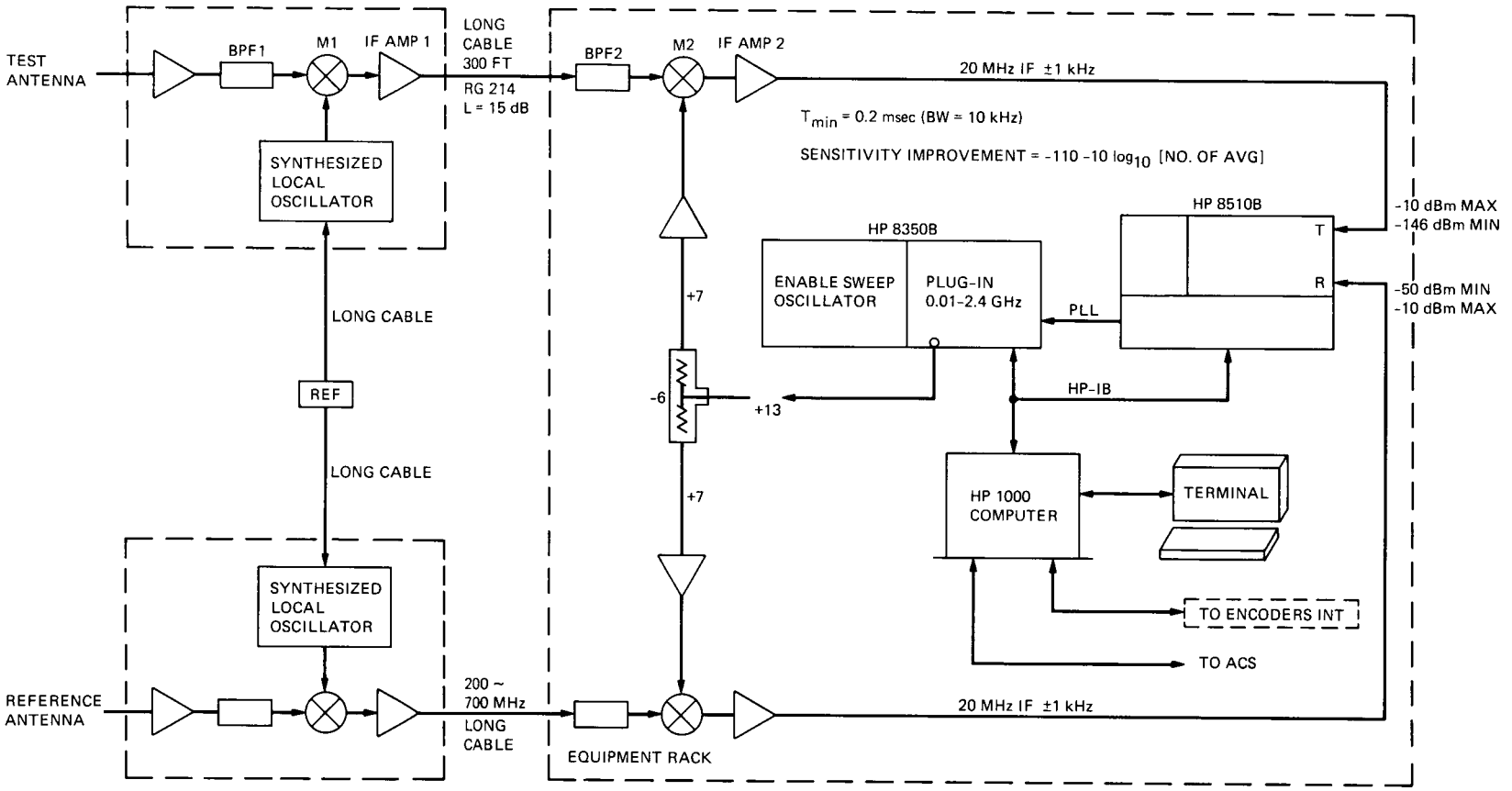


Fig. 2. Block diagram of narrow-bandwidth holographic measurement system.

ORIGINAL PAGE
COLOR PHOTOGRAPH

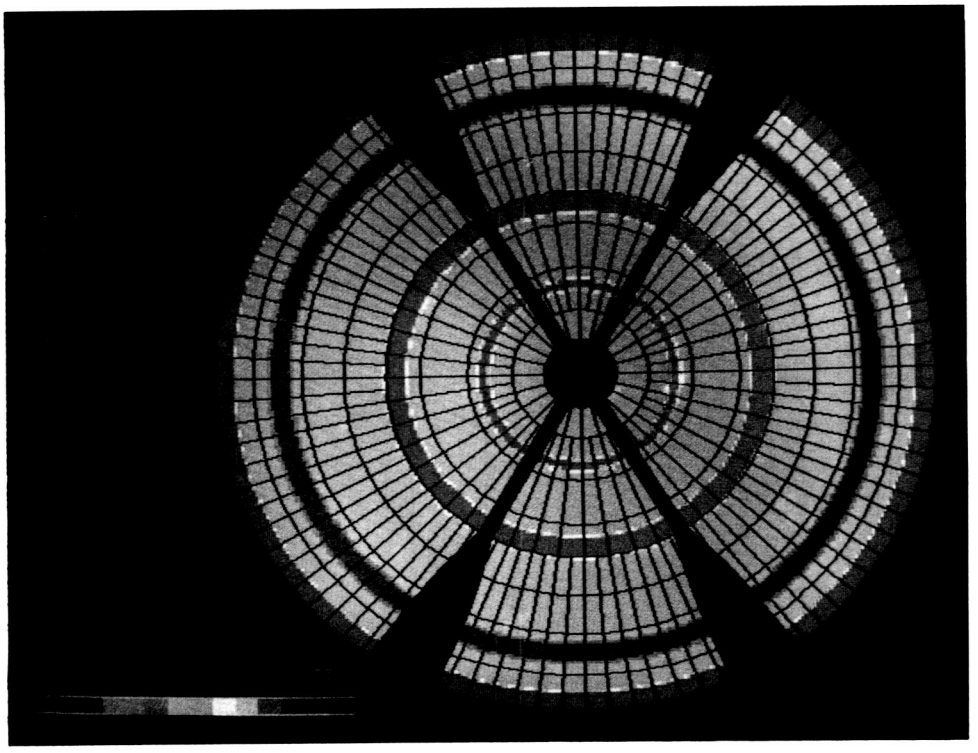


Fig. 3. Surface error map for the parameters in Table 2, No. I.

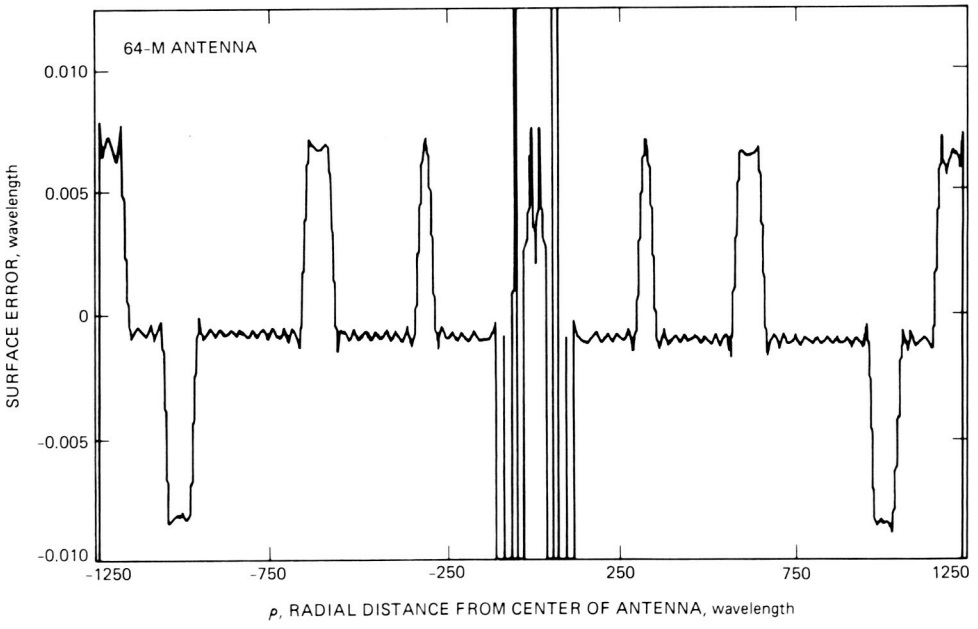


Fig. 4. Cut plot of No. I.

ORIGINAL PAGE
COLOR PHOTOGRAPH

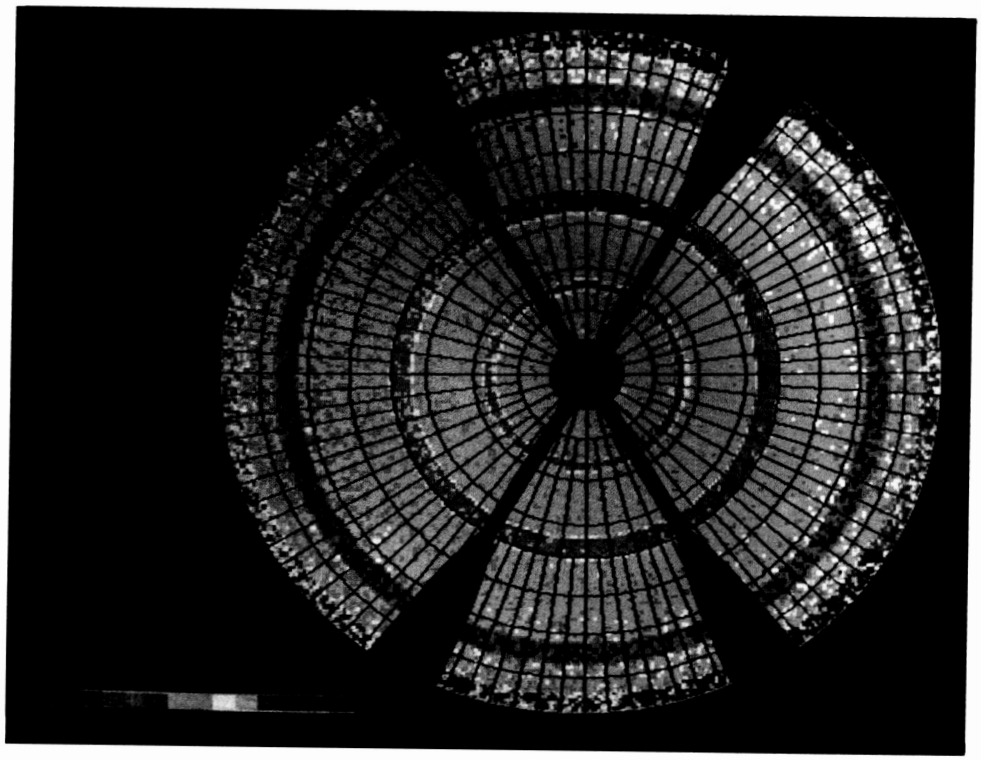


Fig. 5. Surface error map for the parameters in Table 2, No. II.

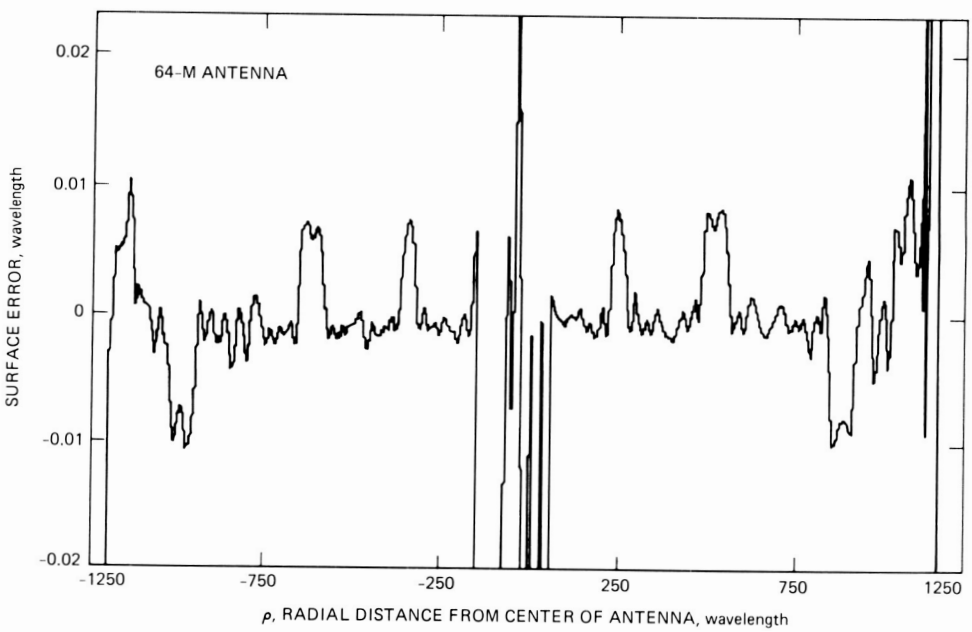


Fig. 6. Cut plot No. II.

ORIGINAL PAGE
COLOR PHOTOGRAPH

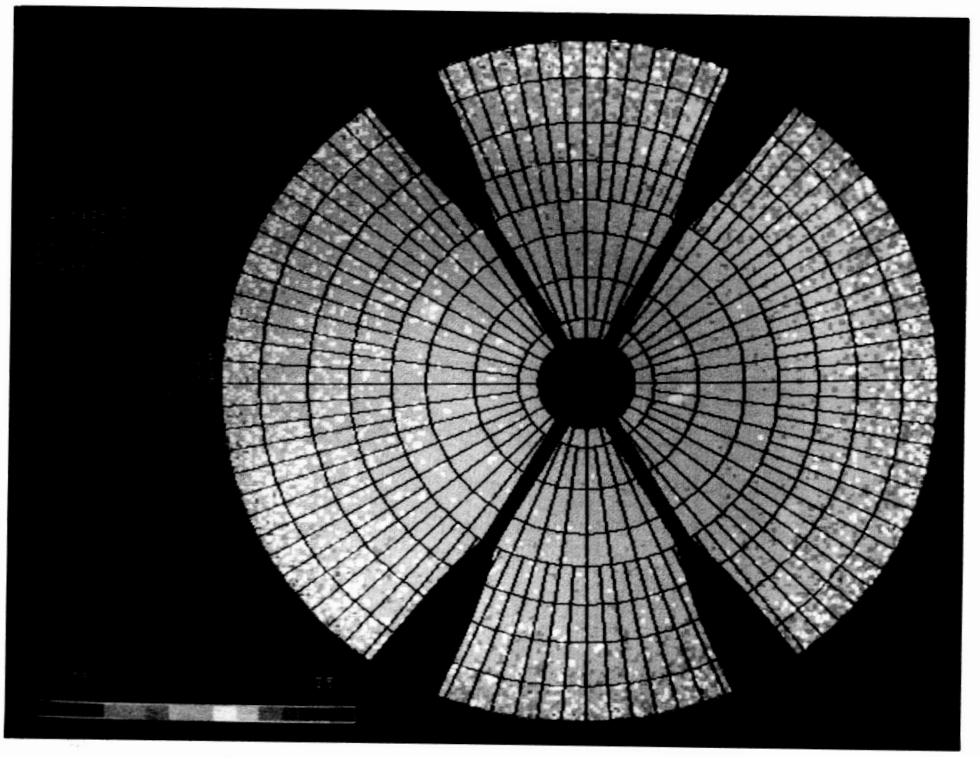


Fig. 7. Map differencing No. II.

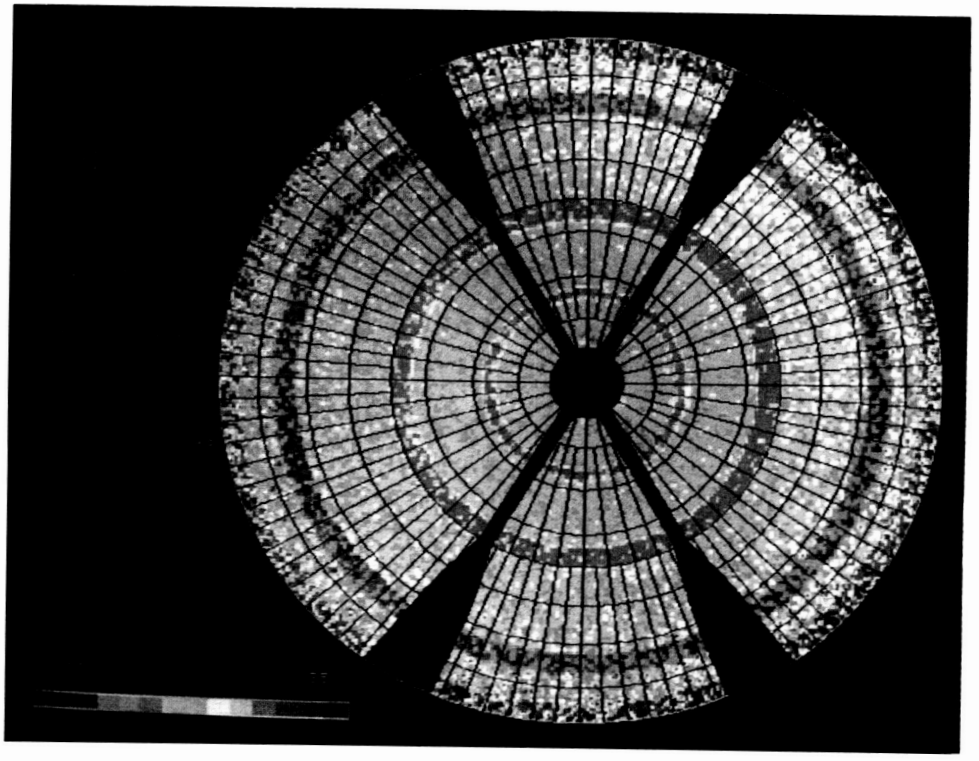


Fig. 8. Surface error map for the parameters in Table 2, No. III.

ORIGINAL PAGE
COLOR PHOTOGRAPH

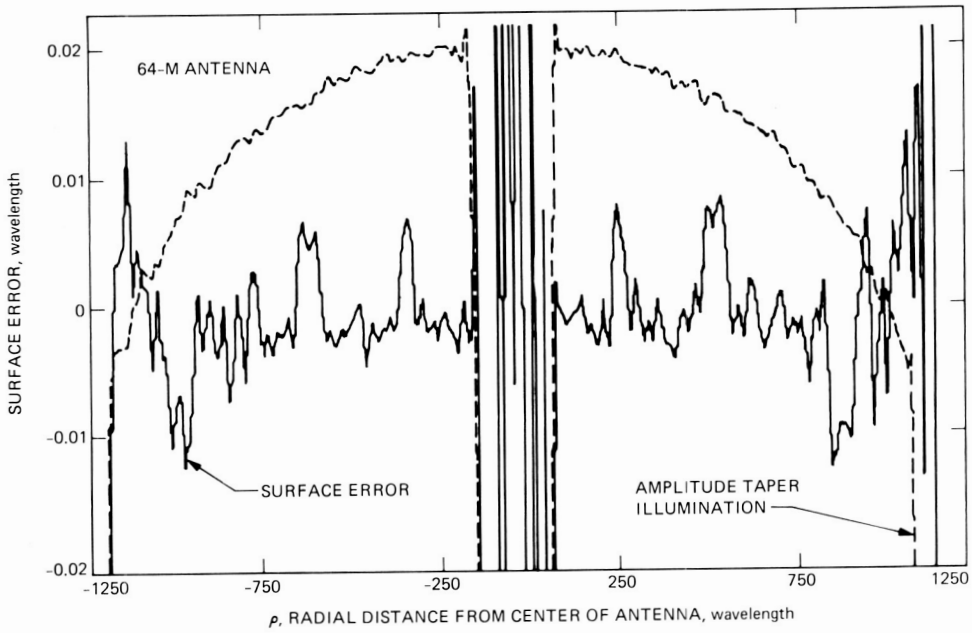


Fig. 9. Cut plot No. III.

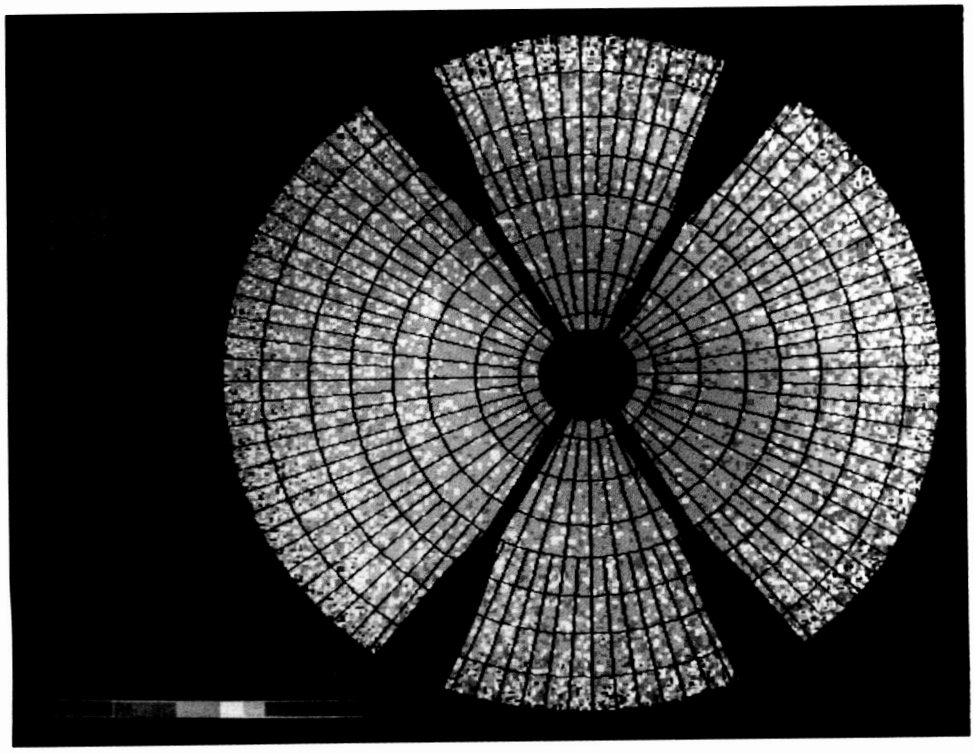


Fig. 10. Map differencing No. III.

ORIGINAL PAGE
COLOR PHOTOGRAPH

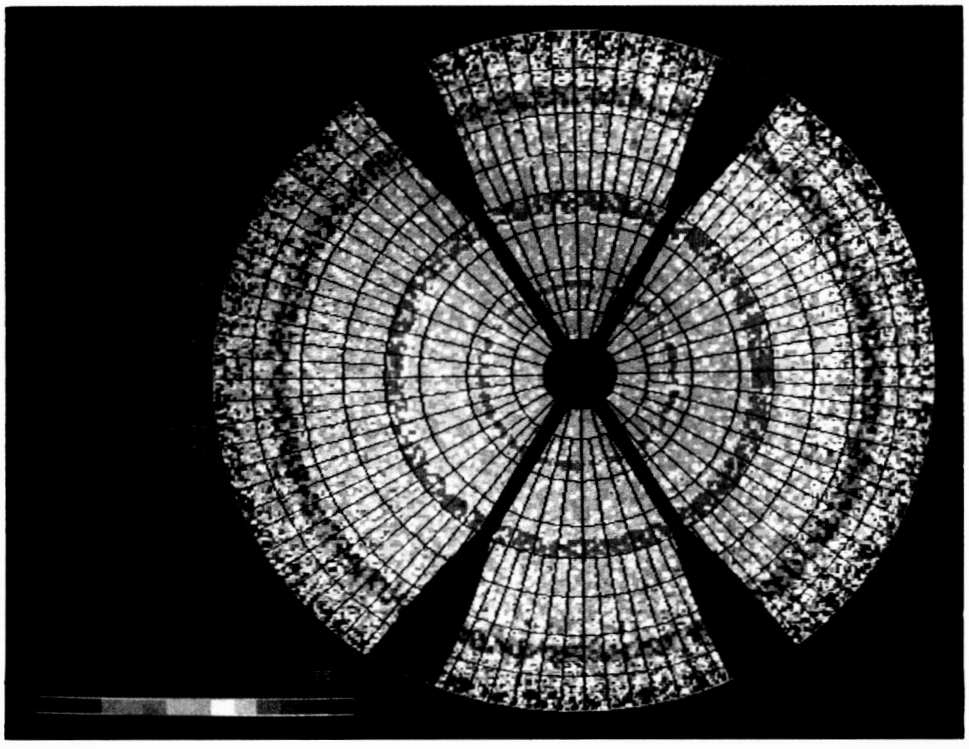


Fig. 11. Surface error map for the parameters in Table 2, No. IV.

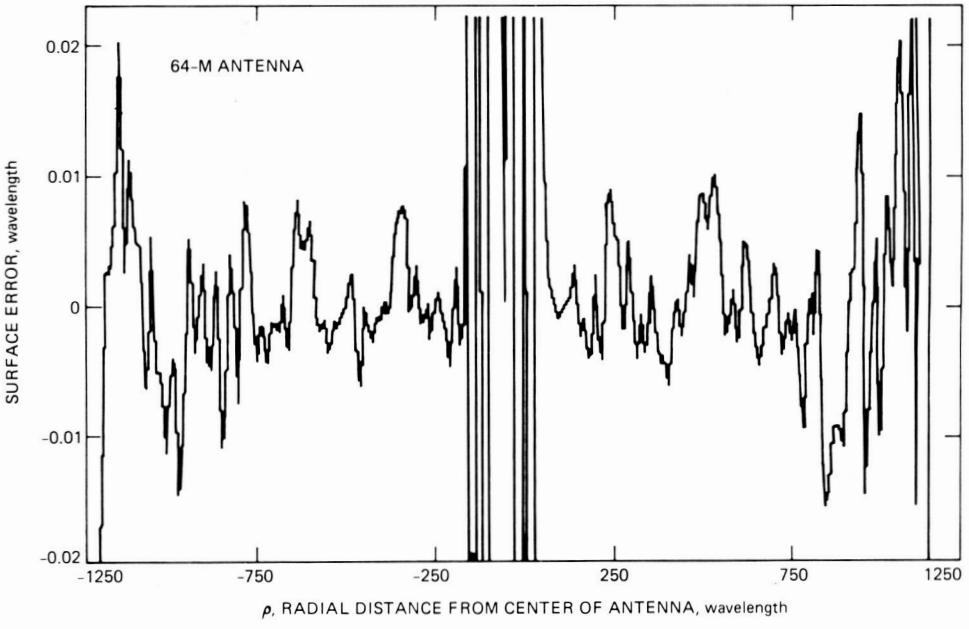


Fig. 12. Cut plot No. IV.

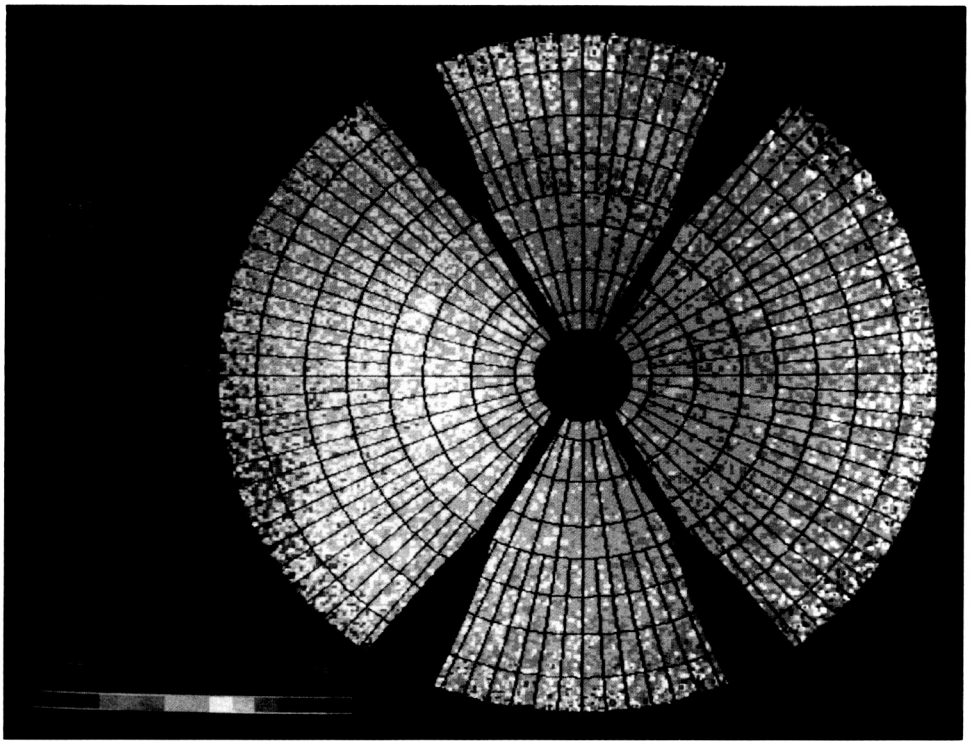


Fig. 13. Map differencing No. IV.

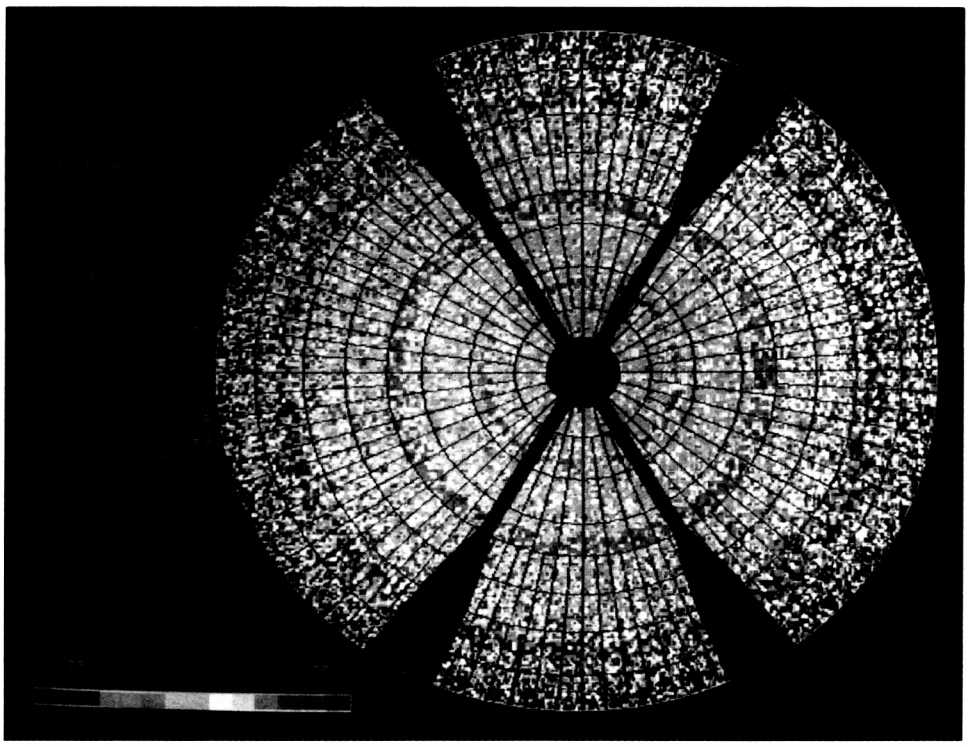


Fig. 14. Surface error map for the parameters in Table 2, No. V.

ORIGINAL PAGE
COLOR PHOTOGRAPH

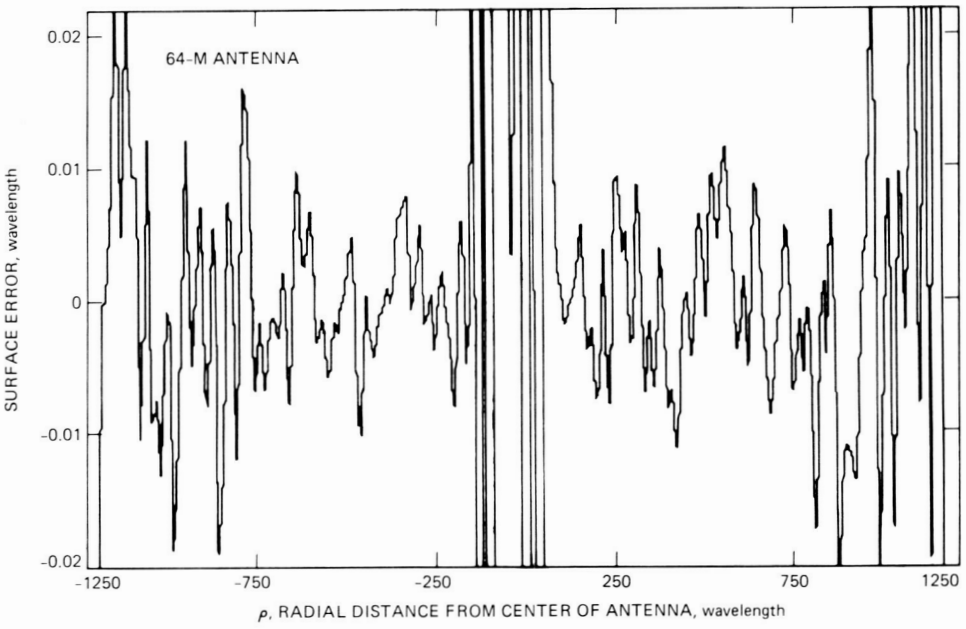


Fig. 15. Cut plot No. V.

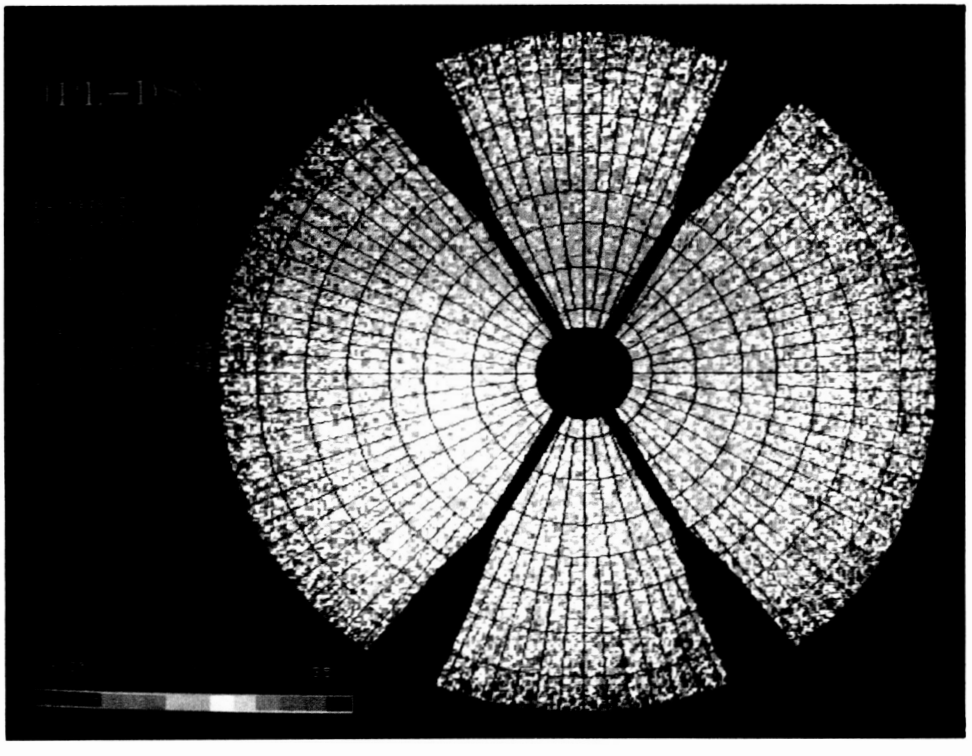


Fig. 16. Map differencing No. V.

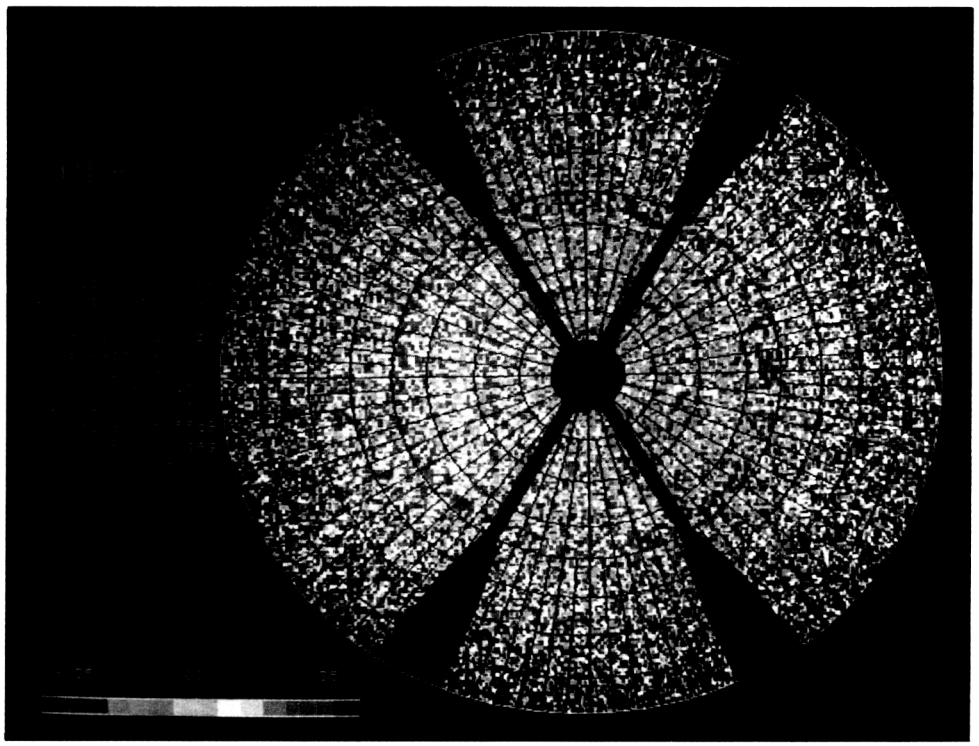


Fig. 17. Surface error map for the parameters in Table 2, No. VI.

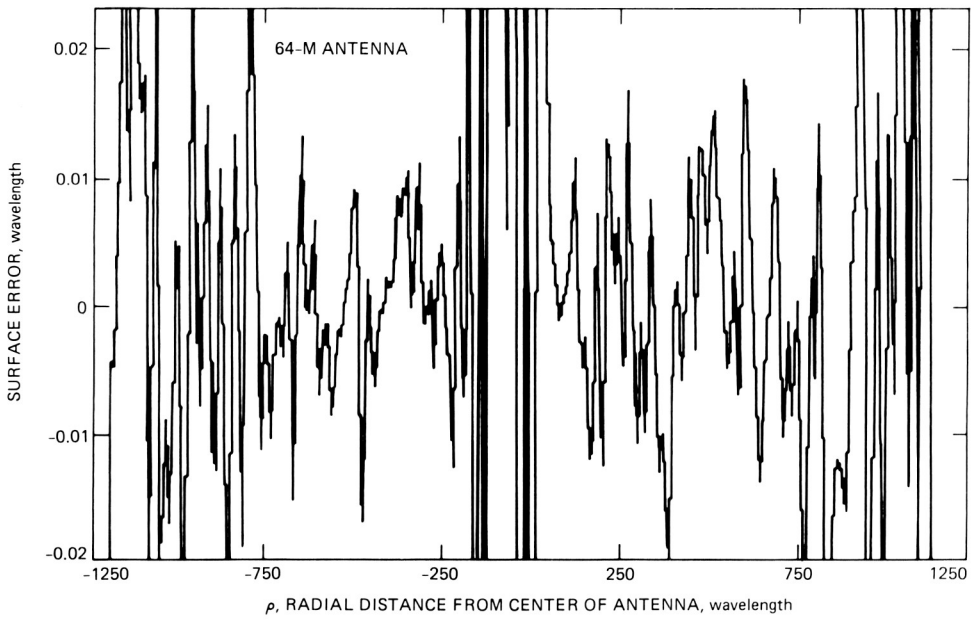


Fig. 18. Cut plot No. VI.

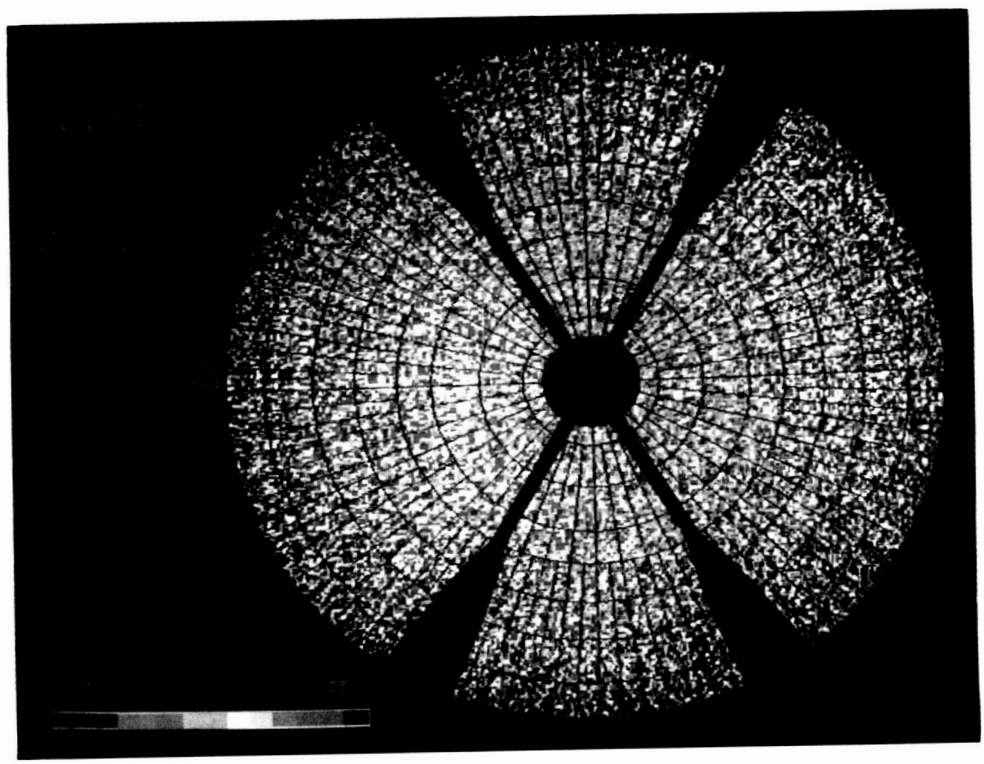


Fig. 19. Map differencing No. VI.

Appendix A

Phase Retrieval Holography Technique

The antenna aperture function $f(x)$ is band-limited to a given range (the antenna diameter).

$$f(x) = 0 \qquad x > d \tag{A-1}$$

(For simplicity of illustration, functions of one variable shall be used without loss of generality.)

For a smooth $f(x)$, the magnitude of the far-field function $F(u)$ will essentially be contained in a band U_{max}. Under these conditions. the Fast Fourier Transform (FFT) is valid and the far-field and aperture-field functions can be related by:

$$f(x) = F^{-1}\{F(u)\} \tag{A-2}$$

and

$$F(u) = F\{f(x)\} \tag{A-3}$$

where F and F^{-1} denote the FFT and IFFT operators, respectively.

For this band-limited function, the Hilbert Transform can be applied:

$$\text{Imag}\, F(u) = H\{\text{Re}\, F(u)\} \tag{A-4}$$

$$\text{Re}\, F(u) = -H\{\text{Imag}\, F(u)\} \tag{A-5}$$

where H denotes the Hilbert transform, and Re and Imag denote the real and imaginary parts of a complex function.

Numerical procedures can now be employed to obtain the phase of $F(u)$ from a knowledge of $|F(u)|^2$, the measured far-field intensity function [9]. Generally, a unique solution will not be obtained, since $F(z)$, $z = x + jy$, is an entire transcendental function and not a finite polynomial.

A transcendental entire function has infinitely many zeros where a zero z_k of $F(z)$ is a solution of

$$F(z_k) = 0 \tag{A-6}$$

which corresponds to an intensity null in the far-field function.

$F(u)$ is the projection on the real axis (of the complex plane) of the entire function $F(z)$, which is encoded by its zeros z_k. Another entire function, $F^1(z)$, which has a flipped zero z_k^* across the real axis, will have the same modules as $|F(u)|$ or

$$|F^1(u)| = |F(u)| \tag{A-7}$$

Therefore, a unique phase solution cannot be obtained without some further information that will allow the removal of phase ambiguity [10].

The additional information required to solve the phase uniqueness problem can be acquired from intensity information of the Geometrical Theory of Diffraction (GTD)-predicted aperture field functions, or previously derived aperture intensity functions from holographic measurements performed at the same measured frequency, i.e., S-band. Figure A-1 demonstrates the excellent agreement between the envelopes of the GTD-predicted aperture amplitude and the actual aperture amplitude derived via holography processing from measured holographic (amplitude and phase) far-field patterns. Reflector and subreflector small misalignments are mostly noticeable in the aperture phase function, while the aperture amplitude function is mostly unchanged. The iterative approach is presented here, while Appendix B presents a minimization in one step. This error-reduction algorithm starts by transforming the aperture complex field to the far field via FFT, replacing the amplitude part by the measured amplitude, then transforming back to the aperture field via IFFT, replacing the amplitude function and repeating the procedure until convergence to a global minimum is reached. This algorithm was suggested by Gerchberg and Saxton [11]. The good initial "guess" promises convergence to the global minimum (see Fig. A-2). This minimum is the square error of the difference between the measured far-field amplitude and the iterated one.

$$E = N^{-2} \sum_{u} [|G_k(u)| - |F(u)|]^2 \tag{A-8}$$

where

N^2 = total number of data points

$|F(u)|$ = measured far-field intensity function (see Fig. A-2)

$|G_k(u)|$ = computed far-field intensity function (see Fig. A-2)

It can be shown, by application of Parseval's theorem, that the square error E will monotonically decrease or stay constant.

Another algorithm suggested by Misell [12] makes use of two measured intensity far-field functions obtained for a focused and a defocused image (subreflector position). This algorithm has been reported to have better convergence, although it is not as attractive as the algorithm presented above. The amount of additional work needed to make a decision is not large.

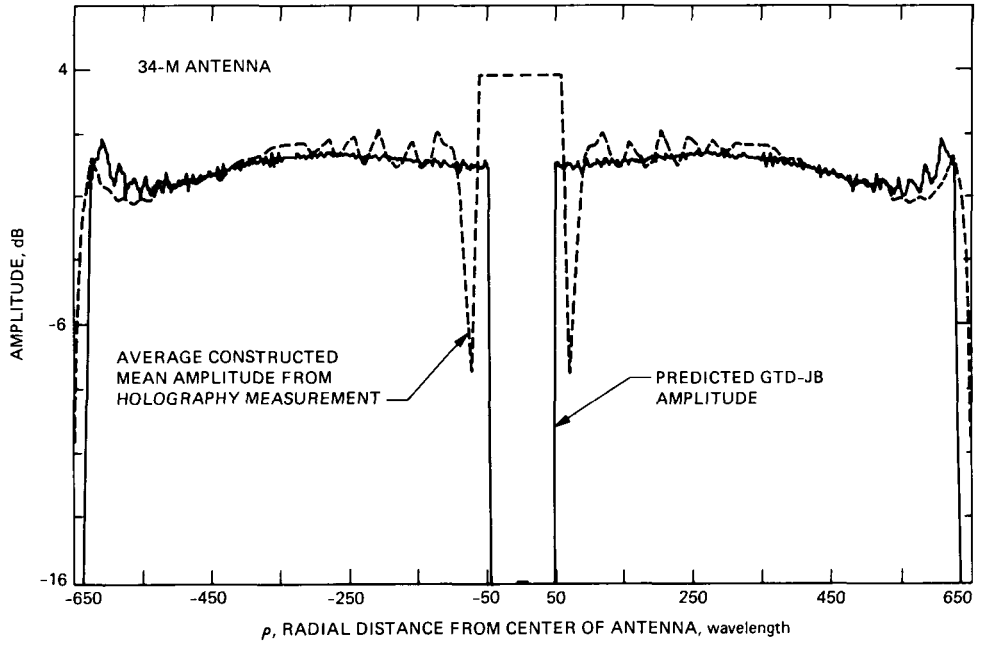
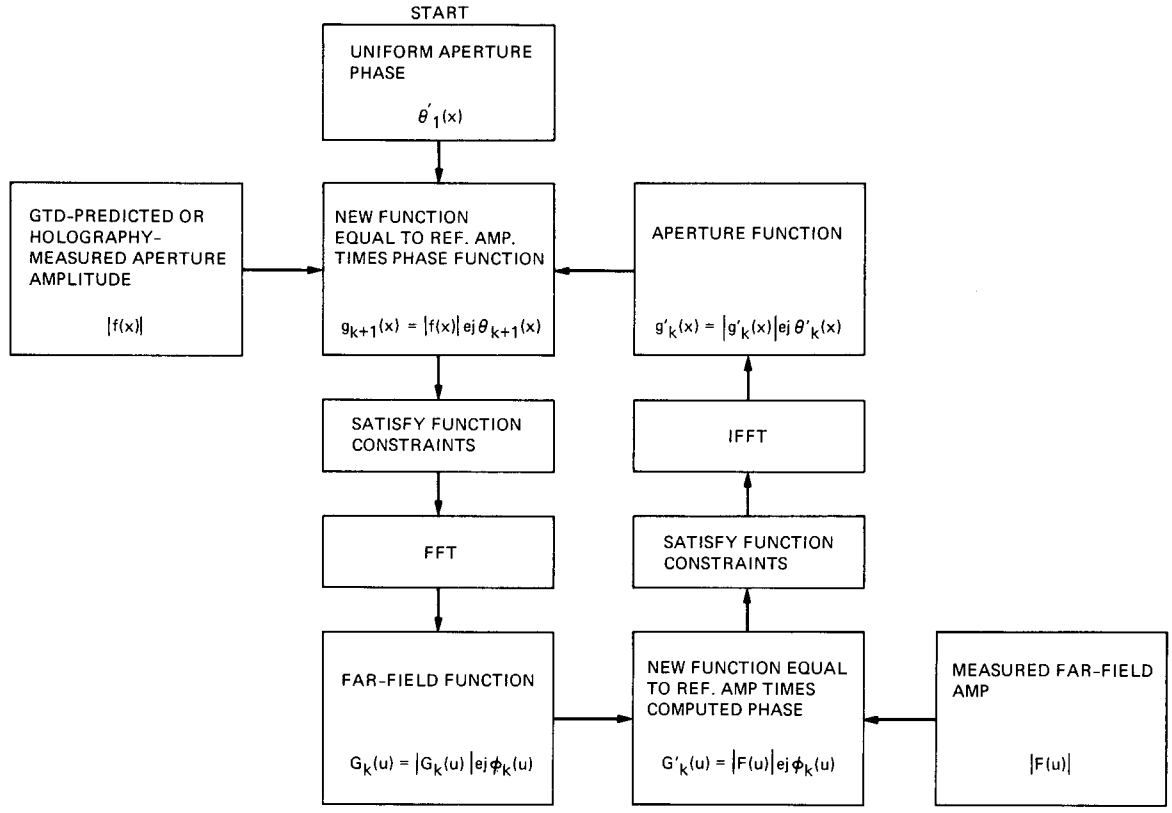


Fig. A-1. A comparison of aperture amplitude functions from GTD-predicted results (solid line) and holographic measurement data (dashed line).



$$G_k(u) = |G_k(u)| \exp[j\phi_k(u)] = F\{g_k(x)\}$$

$$G'_k(u) = |F(u)| \exp[j\phi_k(u)]$$

$$g'_k(x) = |g'_k(x)| \exp[j\theta'_k(x)] = F^{-1}\{G'_k(u)\}$$

$$g_{k+1}(x) = |f(x)| \exp[j\theta_{k+1}(x)] = |f(x)| \exp[j\theta'_k(x)]$$

Fig. A-2. Phase retrieval (error reduction) algorithm after Gerchberg and Saxton [11].

Appendix B
Minimization Technique for Phase Retrieval Holography

The minimization technique suggested here (by Galindo and Rochblatt) will solve for the antenna aperture phase in one step, thus eliminating the iterative approach discussed in Appendix A.

This derivation assumes that the ideal antenna aperture amplitude function $A_I(x)$ is unchanged by small reflector and subreflector misalignments, and that the phase change $\delta\theta(x)$ due to those misalignments is small. These are assumptions inherent in the holographic technique in any case. The "smallness" of the aperture phase error $\delta\theta(x)$ may or may not be more stringent here.

For simplicity, all equations are derived in one dimension without loss of generality (to the two-dimension case).

Let the ideal antenna aperture function be

$$f_I(x) = A_I(x) \exp [j\theta_I(x)] \tag{B-1}$$

and the actual aperture function be

$$f(x) = A(x) \exp [(j\theta(x))] \tag{B-2}$$

The actual far-field function can now be related to the aperture function by a Fourier Transform integral:

$$F(u) = A_F(u) \exp [j\phi(u)] = \int_x A(x) \exp [j\theta(x)] \exp [-jkux] \, dx \tag{B-3}$$

Using the aperture amplitude approximation implies

$$A_I(x) \approx A(x) \tag{B-4}$$

and for the phase

$$\theta(x) = \theta_I(x) + \delta\theta(x) \tag{B-5}$$

and for small $\delta\theta(x)$

$$\exp [j\theta(x)] \approx \exp [j\theta_I(x)] \, [1 + j\delta\theta(x)] \tag{B-6}$$

It is this linearization, Eq. (B-6), of the phase error function that permits the "one step" solution for $\delta\theta(x)$.

Note that a small phase error $\delta\theta(x)$ will invariably justify the $A_I \approx A$ approximation, Eq. (B-4). Thus, the far-field function can be written

$$F(u) \approx \exp [j\theta_I] \int_x A_I(x) \, [1 + j\delta\theta(x)] \exp [-jkxu] \, dx \tag{B-7}$$

where the ideal aperture phase $\theta_I(x)$ was taken as a constant (the usual situation, or it could be taken as a known function of x). Thus

$$F(u) \approx A_{FI}(u) \exp [j\phi_I(u)] + j\exp [j\theta_I] \times \int_x A_I(x) \, \delta\theta(x) \exp [-jkxu] \, dx \tag{B-8}$$

where $A_{FI}(u)$ and $\phi_I(u)$ are the ideal far-field functions.

The aperture phase error can now be represented, in general, by

$$\delta\theta(x) \equiv \sum^{N} a_n g_n(x) \tag{B-9}$$

where $g_n(x)$ is the comb function and the a_n are real coefficients. Equation (B-8) can now be written

$$F(u) \approx A_{FI}(u) \exp [j\phi_I(u)] + j\exp [j\theta_I] \times \sum^{N} a_n \int_x A_I(x) g_n(x) \exp [-jkxu] \, dx \tag{B-10}$$

Equation (B-10) presents the antenna far-field function as a sum of the far-field ideal function (perfect antenna) plus the residual errors (in both amplitude and phase) introduced by the residual phase errors in the antenna aperture.

The coefficients a_n are found by minimizing the square error function E (see Appendix A) over the field of far zone positions u.

$$E = N^{-2} \sum_{u} \left\{ |A_F(u)|^2 - \left| A_{FI}(u) \exp\left[j\phi_I(u)\right] + j \exp\left[j\theta_I\right] \sum^{N} a_n \int_x A_I(x)\, g_n(x) \exp\left[-jkux\right] dx \right|^2 \right\} \tag{B-11}$$

where $|A_F(u)|^2$ is the measured antenna far-field intensity.

$$E = f(a_1, a_2, \ldots a_n) \tag{B-12}$$

The function E has a quadratic form and the minimization of Eq. (B-11) can thus be done in one step using a standard Newton-Raphson method. Note that the gradient and the Hessian matrices are readily found from the same function evaluations of

$$\int_x A_I(x)\, g_n(x) \exp\left[-jkux\right] dx$$

In essence, the solution for the unknown a_n or $\delta\theta(x)$ is found in closed form.

Ka-Band Study—1988

J. W. Layland
TDA Planning Office

R. L. Horttor
Telecommunications Systems Section

R. C. Clauss and J. H. Wilcher
TDA Technology Development Office

R. J. Wallace
TDA Engineering Office

D. J. Mudgway
TDA Mission Support and DSN Operations Office

The Ka-band study team was chartered in late 1987 to bring together all the planning elements for establishing 32 GHz (Ka-band) as the primary downlink frequency for deep-space operation, and to provide a stable baseline from which to pursue that development. This article summarizes the results of that study at its conclusion in mid-1988, and corresponds to material presented to NASA's Office of Space Operations on July 14, 1988. For a variety of reasons, Ka-band is the "right" next major step in deep-space communications. It offers increases in the downlink telemetry capability on the order of 6 to 10 dB. It offers improved radio metric accuracy through reduced plasma sensitivity and increased bandwidth. Because of these improvements, it offers the opportunity to reduce costs in the flight radio system or in the DSN by allocating part of the overall benefits of Ka-band to this cost reduction. A mission scenario is being planned that can drive at least two and possibly all three of the DSN subnets to provide a Ka-band downlink capability by the turn of the century. The implementation scenario devised by the study team is believed to be feasible within reasonable resource expectations, and capable of providing the needed upgrade as a natural follow-on to the technology development which is already underway.

I. Introduction

The Ka-band study team was chartered in late 1987 to bring together all the planning elements for establishing 32 GHz (Ka-band) as the primary downlink frequency for deep-space operation, and to provide a stable baseline from which to pursue that development. A working premise for the study was that the DSN should have full Ka-band downlink services available on the 70-meter and both 34-meter subnets by the year 2000. That premise was examined during the study and found to be consistent with an optimistic view of potential flight missions, and found to be achievable under resource assumptions consistent with that mission scenario.

The work of the study coalesced on schedule as a top-level plan for establishing Ka-band in the DSN. It was presented, after suitable JPL review, to NASA's Office of Space Opera-

tions on July 14, 1988. The final report[1] documents the study results and plan as of the date of that presentation. The report spans the full range of the study effort, from technology development to operations considerations, and from mission requirements to selection rationale for various potential implementation scenarios. This article is a subset of the material to be found in the study's final report, providing a brief summary which emphasizes the nearer-term aspects of the planning for evolution to Ka-band. Readers interested in greater depth should refer to the final report and thence to the many references catalogued there.

Advantages of the higher frequency accrue to both telemetry and radio metric services. For telemetry, there is an anticipated increase in channel capability of 4 to 10 times due to the better directing of energy for assumed fixed sizes of antenna. This is mitigated somewhat by the uncertainties that exist today in weather-induced attenuation and system noise, and in component efficiencies. These uncertainties drive much of the technology development work discussed later in this article.

For radio metrics, the higher frequency means less sensitivity to plasma-induced errors, and hence higher precision for both navigation and many radio science measurements. In addition, the wider allocated bandwidth of 500 MHz could be used to support more accurate delay/range measurements. On the flight mission side, some of these benefits can be traded for reductions in antenna size or transmitter power, facilitating the construction of some very constrained mission elements such as a Mars rover.

A baseline plan for the evolution to higher frequencies exists in broad form and is documented in the current DSN Long-Range Plan and the 1987 Construction of Facilities Plan. The technology base upon which to build has been documented in part in the special Ka-band issue of the *TDA Progress Report* [1], and in a plethora of other scattered reference material. These elements formed the background against which to pursue the team's planning activities and with which to focus the necessary analysis.

II. Network Performance and Mission Benefits

The performance of the 70-meter antenna at Ka-band was predicted prior to its construction, as shown in Fig. 1.[2] Measurements of the actual 70-meter Ka-band performance baseline are yet to be done. Technology work needed to achieve the higher levels of performance form a part of technology development planning to be discussed later in this article. The predicted Ka-band performance of the 34-meter antenna is shown in Fig. 2. This performance was based on analytical work done in May 1988 by D. Bathker.[3]

The value of Ka-band to a specific mission depends upon several variables in addition to ground antenna gain. These include receiver noise temperature, atmospheric attenuation and noise temperature, pointing accuracy, downlink power, etc. Atmospheric effects depend upon the randomly varying weather as well as viewing geometry. Link performance is thus dependent upon the spacecraft position in the sky. Figure 3 is a typical telecom prediction curve for the data rate achievable at 90 percent confidence from a spacecraft at equatorial declination, using either Ka-band or X-band, with 21 watts RF power and a Voyager-size 3.66-meter antenna.[4] These curves are based upon current best understanding of the weather model[5] and Ka-band device behavior, coupled with the optimized Ka-band performance depicted in Fig. 1.

The proposed Cassini mission consists of a Saturn orbiter carrying a probe for the atmosphere of the satellite Titan. In a very real sense it is a Galileo mission at Saturn instead of Jupiter and, hence, at significantly greater distance from Earth. The decrease in signal strength due to this greater distance could be comfortably compensated for by switching the downlink from X-band to Ka-band, thus making Cassini one of the several candidates for DSN Ka-band services.

Early in 1988, the Cassini preproject teams concluded a Science Data Return Study[6] which analyzed in detail a number of possible downlink options. They observed that a Ka-band 3-watt downlink could return all the expected baseline science instrument data, but was not yet technologically mature enough to be selected as the primary downlink. Other improvements to the downlink performance, such as the new long constraint length convolutional code to be flown experimentally on Galileo [2] or improvements to the DSN X-band receiving performance (to be discussed later in this article), could also satisfy the data transfer needs as long as the science data load does not grow above currently estimated levels.

---

[1]J. W. Layland et al., *Ka-Band Study–1988, Final Report*, JPL Publication D-6015, Project Document 890-212 (internal document), Jet Propulsion Laboratory, Pasadena, California, January 15, 1989.

[2]R. L. Horttor, editor, *Ka-Band Deep Space Communications*, JPL Publication D-4356 (internal document), Jet Propulsion Laboratory, Pasadena, California, p. 26, May 15, 1987.

[3]D. Bathker, private communication.

[4]Horttor, op. cit., pp. 15–30.

[5]Ibid., pp. 60–65.

[6]D. Collins et al., "Cassini Science Data Return Study," presentation viewgraphs (internal document), Jet Propulsion Laboratory, Pasadena, California, January 1988.

The Mars Rover Sample Return mission is another candidate future mission that could benefit significantly from the adoption of Ka-band as its primary downlink frequency. The added link performance enables use of higher data rates, allowing wider travel by the rover supported by the rapid communication of guidance information from Earth. Part of the Ka-band advantage can simultaneously be allocated to enable use of a smaller rover antenna size that is lighter in weight and fits conveniently into the carrier vehicle. It also enables routine support from the 34-meter DSN antennas instead of competing for more limited 70-meter antenna time.

A third candidate mission that would benefit from Ka-band is the Solar Probe, which will approach within four solar radii of the Sun's surface to perform its scientific measurements. X-band communications can provide neither an adequate science telemetry return through the solar corona nor Doppler accuracy to 0.1 mm/sec for the gravity field measurement. A two-way Ka-band link together with X-band as a calibration signal appears to be the best way to achieve the accuracies that are required to meet the celestial mechanics objectives for the mission.

III. Main Building Blocks and Options

It is apparent that there are mission scenarios for which any or all of the DSN subnets will be required to be Ka-band-capable by the end of this century. Each of the three current (1988) DSN subnets has been examined to determine its potential at Ka-band and to define the principal configuration options for each. On the old 34-meter "standard" subnet, the structure and surface quality are totally inadequate for use at the 32-GHz Ka-band frequency. Replacement of the 34-meter standard antenna appears to be the only realistic option for providing any of several added capabilities, including Ka-band, on this subnet. By way of contrast, the much newer 34-meter "high-efficiency" (HEF) subnet is thought to have adequate structural stiffness and surface quality to provide reasonable Ka-band efficiency. The microwave feed area, however, is essentially filled with equipment providing current services, and needs to be totally reconfigured to make room for any new services. A similar story holds for the newly enlarged 70-meter antenna, in that a reasonable level of Ka-band performance should be attainable without significant structural changes. A rigorous program of antenna calibration will be required to attain the expected peak level of performance from the large antennas. This calibration will provide improved beam pointing and automatic compensation for surface distortion and beam deflection due to gravity, thermal effects, and wind load.

Consideration of Ka-band in the DSN cannot stand alone, because most of the present frequency capabilities need to be retained for the foreseeable future. Support of the Pioneers using S-band uplinks/downlinks will continue as long as these spacecraft remain functional. Support of the Voyagers using S-band uplinks/SX-band downlinks will also continue well into the next century while these spacecraft cruise through previously unexplored regions of the outer solar system. With its delayed launch, the Galileo prime mission has been deferred into the latter half of the 1990s and could easily operate past the turn of the century. Galileo requires X-band downlink performance at least equal to the best available today, and responds to an S-band or X-band uplink. Table 1 summarizes the current, forecast, and other known potential frequency-band support requirements on the DSN for the next decade. Essentially all current capabilities will need to be retained at a technical performance level equal to or better than current performance while the addition of Ka-band is made to support the new missions.

The option menu for potential configuration changes to the three deep-space subnets of the DSN is catalogued in Table 2. Conceptual design for each of these was carried out with support from the Ground Antenna and Facilities Engineering Section and the Radio Frequency and Microwave Subsystems Section. A discussion of the entire option set appears in the final report.[7] Only a selected subset appears in this article. Configuration drawings for the antenna mechanical elements described here were provided by the Ground Antenna and Facilities Engineering Section.[8] While much has been learned in the examination of these options, there is still much to be learned about the process of designing for Ka-band and beam waveguide. Experience gained through the design and installation of the new advanced development antenna at DSS-13 should provide that knowledge.

Replacement of the 34-meter standard antenna is driven by several needs: Ka-band downlink for deep space use, X-band uplink with SX-band downlinks, Ku-band for support of the proposed Quasat mission or others in the class of Earth-orbiting interferometry terminals, and C-band for potential cooperative support to Soviet missions. Still another need is for continued reliable support (and modest performance improvement) at the existing S- and X-band channels. These older antennas were built in the early 1960s as 26-meter antennas, and are simply nearing the end of their productive lives. Two replacement options were considered to enable installation of Ka-band capability: an HEF antenna like DSS-15 with all microwave equipment mounted in a cone structure in the antenna dish,

[7]Layland et al., op. cit.

[8]R. Van Hek et al., *Ka-Band Study Plan for the Antenna Mechanical Hardware* (internal report), Ground Antenna and Facilities Engineering Section, Jet Propulsion Laboratory, Pasadena, California, April 1988.

and a centerline beam waveguide antenna like the new DSS-13 with the feeds and related equipment in a nonmoving area in the pedestal (Fig. 4). Of the two, the HEF-type antenna is more completely understood by those who will ultimately have to do the implementation, while the beam waveguide design appears to offer the best flexibility and opportunity for growth to meet future needs.

In addition to providing space for future growth, the nonmoving aspect of the equipment area of the beam waveguide antenna enables technical performance improvement for X-band as well as Ka-band. Because it does not have to tilt, the cryogenic cooler for the low-noise traveling-wave maser amplifier can be made to operate at below atmospheric pressure, permitting a device temperature of around 1.5 kelvins (versus 4.5 kelvins today), and a consequent reduction in system temperature. Also, in the larger space available, the entire feed system can be cooled to 15 kelvins or below, thereby greatly reducing another source of thermal noise. These steps were assumed to be achieved in deriving the predicted performance curves for Ka-band presented earlier. Using Ka-band without these steps would surrender about 1.5 dB of the predicted performance. Updating the X-band system to the potential apparent in a beam waveguide design offers improvements on the order of 2 to 3 dB over current capabilities. The beam waveguide design also can be expected to improve the maintainability of the front-end equipment by virtue of the easier access and nontilting environment.

Taken together, this set of considerations forms a strong argument that any newly constructed antennas in the DSN should incorporate the beam waveguide design. This same set of considerations also applies to any major upgrade of the feed and microwave area of existing antennas, but the associated costs are a counteracting force and the decision process correspondingly less clear. The advantages of the beam waveguide configuration can be obtained for the current HEF antennas by modifying them as shown in Fig. 5.

The option set for the 70-meter antenna is more complicated because it carries a greater variety of services today. The current structure consists of a three-layer stack of cylindrical shells topped by three microwave cones whose mechanical structure is the same as that of the single cone on the smaller antennas. Equipment is mounted in all layers. Two of the three cones provide current S- and X-band services to spacecraft. The third cone provides host-country radio astronomy, the Goldstone Solar System Radar, and technology development support. Virtually all extant services must be preserved in any upgrade of this antenna. Installing Ka-band in one of the cones appears feasible, but with the likely performance penalty noted above, and there is still concern for available space. The space concern can be alleviated for the 70-meter by replacing the selected cone with a one-third pie wedge occupying the same footprint on the supporting structure. Eventually all three cones would be replaced resulting in what has been termed the monocone configuration.

An intermediate option for the 70-meter has been termed the "hybrid" or partial beam waveguide. This option was conceived as a way to obtain the benefits of beam waveguide for Ka-band operation at a modest cost and without risk of degradation to services provided at S-band. For the hybrid option, the two cones providing current spacecraft support remain as they are, thereby retaining current performance levels needed for the Pioneers, the Voyagers, and Galileo. The third cone is removed and replaced with a mirror. The mirror directs the microwave beam into a bypass-style beam waveguide path to an alidade-mounted equipment room providing radio and radar astronomy functions and the new capabilities for Ka-band downlink and X-band uplink services to newer spacecraft. Retaining the cones and adding the beam waveguide requires that the focal length of the subreflector be retained as is, adding one more constraint to the design of the beam waveguide. Figure 6 illustrates one version of the hybrid beam waveguide concept.

IV. Ka-Band Technology and Environmental Effects

Many elements of the DSN and its surrounding environment affect 32-GHz (Ka-band) system performance much more than lower microwave frequencies now in use. Table 3 lists virtually all these elements, including the Earth's ionosphere, following a signal through the stratosphere and troposphere to its arrival at Earth and capture by the DSN. This table forms a menu for meditation, study, analysis, testing, and development to begin the process of getting the DSN ready for the support of missions using Ka-band. Many of these elements have been studied or are currently under study within the DSN Advanced Systems Program; details of the planned efforts can be found within the current Research and Technology Operating Plans (RTOPs).

Knowledge of antenna performance at Ka-band requires careful measurement at or near the actual operating frequencies. Achieving the desired level of performance is expected to require careful adjustment of the antennas as well. The program of holographic measurements to accurately adjust the antenna surface will therefore grow in importance.

On the 70-meter antenna at least, structural deformations due to gravity loading at differing elevation angles or due to wind loading could easily require active compensation to achieve full efficiency at Ka-band. For the purposes of plan-

ning, a seven-element array feed was assumed necessary and sufficient.

DSN antennas are used in a limited fashion at 22 GHz for radio astronomy; measurements at 22 GHz can help predict performance at 32 GHz. Measurements at the 44-GHz astronomy band could enable interpolation to refine our expectations for the 32-GHz behavior of the 70-meter antennas. A fully definitive answer, of course, will not be available until these antennas are instrumented at the 32-GHz Ka-band deep-space communications frequency. Preliminary microwave radiometry measurements should occur next year under currently proposed technology development activities. Installation of a fully capable Ka-band low-noise system is not now scheduled to occur prior to 1995.

A realistic test and demonstration of Ka-band deep-space performance comes with the Ka-band Link Experiment on Mars Observer (KABLE). A key element of this experiment is the simultaneous comparison of X-band with Ka-band signals emanating from a deep-space vehicle. DSN support to KABLE will be from the new advanced development antenna at DSS-13. On the spacecraft, KABLE is a simple quadrupler inserted parallel to the X-band path on the high-gain antenna (HGA). The resulting 33.6-GHz signal is out of the Ka-band space research band, but the low power density at Earth makes the experiment in conformance with radio regulations. However, the frequency is sufficiently close to the allocation for engineering measurements of link performance to be made. The quadrupler was the least costly spacecraft implementation option for the KABLE experiment. Implementation for committed mission support will induce more extensive changes to the flight hardware design.

Figure 7 shows the flight hardware elements necessary for utilization of Ka-band. Central to all is the deep-space transponder, which is only indirectly a Ka-band issue since a transponder is needed in any case. Certain performance requirements become more stringent if a Ka-band downlink is required, but irrespective of Ka-band, a new transponder must be developed for missions in the mid- to late 1990s. The transponder that Mars Observer procures may or may not be adequate for the new Ka-band-compatible transponder. The baseline deep-space transponder will have been designed for two-way X-band.

Two means of power amplification (Fig. 7) are considered options for Ka-band future application. The Ka-band solid-state array feed power amplifier (AFPA) depends on the development of new devices. The chief virtue of the AFPA is near lossless RF signal combining, because the RF signal combines directly at the focal point. Traveling-wave-tube amplifiers (TWTAs) are needed for applications where DC power is particularly constrained, or where substantial RF power is required and radiation into antenna apertures can be achieved without excessive ohmic losses.

V. Implementation Scenario

Planning for major implementation for the DSN involves fitting the required activity into a time-constrained resource box. The beginning of the applicable time interval is defined by the availability of technology needed. The end of that interval is terminated by the delivery date for the required capability to support a mission. The box is further constrained by the limited out-of-service times allowed because of the need to support other missions which are already in flight. Figure 8 is an overview schedule showing the constraining and potentially driving missions and the target dates for the technology program, together with the favored Ka-band implementation scenario which is discussed in this article. This schedule defines a capability to meet the potential need dates of the missions currently in the preplanning stage. As the details of that future mission set evolve and solidify, the specifics of the Ka-band implementation scenario in the DSN will evolve to meet the agreed-upon needs of the customers' missions.

As a first step in the implementation, the DSN would equip a 34-meter subnet for cruise-mode support of CRAF/Cassini with X-band uplink/XKa-band downlink services by mid-1995. This capability would be available on at least two stations at CRAF launch and on the full subnet before Cassini launch. Support to the existing missions—Galileo, Magellan, Mars Observer, and others already in flight—limits the downtime windows available for network changes and constrains the options for installing Ka-band on existing subnets to those that can be accomplished with extremely brief downtimes. Specifically allowed would be replacement of the 34-meter standard (34-STD) subnet, or swapping the cone-module on the 34-meter high-efficiency (34-HEF) subnet. To meet the target schedule and distribute the effort over time, the construction funding should be embedded in the FY'91, FY'92, and FY'93 Construction of Facilities budgets, which will be defined during the 1988–1990 planning cycles.

The preferred configuration for the first 34-meter Ka-band subnet would be the replacement for the 34-STD subnet, using a center-fed beam waveguide antenna design derived from that of the new DSS-13 antenna. The basic antenna system would provide all services currently provided by the 34-STD subnet. To this would be added X-band uplink and then Ka-band downlink capabilities. Considering the space available in this type of structure, installation of Ka-band should be a simple

"drop-in" process, after the technology surprises have been met and conquered at DSS-13. The space and configuration also eases the way for future additions of Ku-band for critical Earth-orbiter support or C-band frequencies currently in use by the Soviet missions. This configuration, with its easy access and nontilting environment, should also reduce future maintenance efforts for the front-end equipment.

The second of the 34-meter subnets capable of X-/XKa-band services is potentially required by the end of 1999 to support the Mars Rover Sample Return (MRSR) mission during its high-activity phases. The configuration choice depends greatly upon the pathway chosen for the first of the 34-meter subnets. If the 34-STD subnet has been replaced and now supports X-band uplink operation, then downtime windows should exist to permit the 34-HEF subnet to be upgraded to a beam waveguide configuration. Only one of the six antennas capable of providing the critical X-/SX-band services would be out of service at any one time. If however, replacement of the 34-STD subnet had been deferred, then its replacement in the 1998–1999 time frame would be the only open option. Construction funding for the available option would be required in FY'97 and FY'98, which means that the decision time for the second 34-meter subnet is actually in the 1995–1996 planning cycle.

Establishing Ka-band on the 70-meter subnet presents its own set of special considerations. These antennas are the largest and most crucial elements of the DSN. Their performance at Ka-band can be the key to outstanding science return from Cassini during its Saturn satellite tour starting in 2003. Because of their very size, they are subject to added technology uncertainties in their pointing and in their structural deformation under gravity, thermal, and wind loading. These uncertainties are not present in the smaller 34-meter antennas. For that reason, it would be prudent to establish a quasi-operational best-efforts Ka-band capability on the Goldstone 70-meter antenna long before becoming committed to a specified level of Ka-band performance on the 70-meter subnet. The actual schedule driver for this capability is the MRSR mission approach to Mars, giving a DSN operational date in mid-1999. The Cassini mission is proposed to fly in 1996.

Installation and demonstration of the prototype 70-meter Ka-band capability at Goldstone prior to Cassini launch is desirable for two reasons. First, it offers a visible demonstration to the project of the intent to provide the Ka-band capability needed for its encounter. Second, it offers enough time for DSN personnel to discover and solve the special 70-meter Ka-band problems not present with the 34-meter, and to do that in time to avoid those problems with the operational configuration. Given current mission shcedules, a downtime window will exist in 1994 which could be used to prepare the antenna configuration as needed. This would require construction funding in FY'93, for which the critical decision point occurs in the 1991–1992 planning cycle.

The preferred configuration for this prototype 70-meter Ka-band installation was described earlier as the hybrid or partial beam waveguide. This configuration retains the cone configuration for the current S- and X-band services without noticeable degradation from their current performance. The added beam waveguide feature would provide for the demonstration of X-/XKa-band services, for research and development efforts of various sorts, and for radio and radar astronomy. If installed on the proposed schedule, the beam waveguide area would provide a place to install a supercooled X-band receive function, which could be demonstrated or used for best-efforts support of Galileo during its arrival at Jupiter. It also could provide a place to install the planned megawatt radar transmitter, without adding weight to the tipping structure of the antenna. Design of the partial beam waveguide would be constrained to facilitate a later upgrade to full beam waveguide when and if that became a correct step.

The full 70-meter subnet would be required to have X-band uplink and X- and Ka-band downlink services by mid-1999. The actual schedule driver as forecast today would be the MRSR approach to Mars, but Cassini's approach to Saturn is not long after this. For now, downtime windows appear to exist in the 1998–1999 time period to permit needed modifications and installation of Ka-band services. Construction funding would be required in FY'97 and FY'98, for which the critical decision time is the 1995–1996 planning cycle. There are three configuration options visible today for this installation, all of which should be well understood by decision time. These three options, all discussed in detail in the final report, are the full beam waveguide, the partial beam waveguide, or the expanded pie-wedge cone module. Experience with DSS-13 and a better understanding of the real mission drivers will facilitate that decision at the proper time.

VI. Conclusion

The conclusions of the Ka-band study effort can be briefly summarized. For a variety of reasons, Ka-band is the "right" next major step in deep-space communications. It offers increases in downlink telemetry capability on the order of 6 to 10 dB. It offers improved radio metric accuracy through reduced plasma sensitivity and increased bandwidth. And because of these improvements, it offers the opportunity to reduce costs in the flight radio system or in the DSN by allocating part of the overall benefit of Ka-band to this cost reduction. Improvement in DSN efficiency and productivity would thereby result from the introduction of Ka-band

operation. And the new capability would maintain and extend the visible NASA lead in deep-space communications.

As described in this article, a mission scenario is in planning which can drive at least two and possibly all three of the DSN subnets to provide a Ka-band downlink capability by the turn of the century. In addition, the implementation scenario outlined here is feasible within reasonable resource expectations, and can provide the needed upgrade as a natural follow-on to the technology development which is already underway. The upcoming development on the new DSS-13 antenna forms a key part of that technology effort.

Acknowledgment

Although the specific form of this report is the result of the Ka-band study team's efforts, the technical foundation for it is a result of significant support by many members of the Telecommunications Division and the Office of Telecommunications and Data Acquisition. Their efforts are gratefully acknowledged.

References

[1] "Ka-Band Capabilities" section, *TDA Progress Report 42-88*, vol. October–December 1986, Jet Propulsion Laboratory, Pasadena, California, pp. 96–172, February 15, 1987.

[2] S. Dolinar, "A New Code for Galileo," *TDA Progress Report 42-93*, vol. January–March 1988, Jet Propulsion Laboratory, Pasadena, California, pp. 83–96, May 15, 1988.

Table 1. DSN frequency band requirements

Service	70-meter antenna	34-meter HEF antenna	34-meter standard and replacement	26-meter antenna
S/S	International Cometary Explorer Pioneer 6-8, 10, 11		AMPTE[a] Pioneer 6-8, 10, 11 ISTP-Wind et al.[b]	AMPTE[a] Earth-orbit launches Earth-orbit emergency Select earth orbit ISTP[b]
S/SX	Galileo Magellan Pioneer 12 Ulysses Voyager Venus Probe[c] Comet Sample Return[d]	Downlink: Pioneer Voyager Galileo	Galileo ISTP-Geotail[b] Magellan Ulysses Voyager Venus Probe[c]	(?) ISTP-Geotail[b]
C/L	Phobos			
C/C	Mars balloon Mars aeronomy Vesta, et al.[e]		Mars balloon (?) et al.	
X/SX	Comet Nucleus Sample Return (?) Galileo, Magellan	Comet Nucleus Sample Return Galileo, Magellan		
X/X	Mars Observer	Mars Observer	Lunar Geoscience Observer	Planetary launches (?) Lunar Geoscience Observer, Mars Observer
X/XKa	Comet Rendezvous Asteroid Flyby Mars Rover Sample Return MBAR, NEAR, SFSP[f] Comet Coma[c]	Mars Rover Sample Return	Mars Observer (demo) Comet Rendezvous Asteroid Flyby Mars Rover Sample Return MBAR, NEAR, SFSP[f] Comet Coma[c]	
X/SXKa	Cassini		Cassini	
Ku/Ku or X/Ku			Quasat Orbital transfer vehicle	Quasat (?) Space station (?)
Ka/XKa	Solar Probe			
Other	GSSR, Host R/A[g]		GSSR, SETI[h]	

[a]Active Magnetospheric Particle Tracer Explorers.

[b]International Solar Terrestrial Physics Programme. Wind is a NASA payload for ISTP. Geotail is a joint NASA-ISAS satellite.

[c]Institute of Space and Astronautical Science (ISAS), Japan.

[d]ISAS-European Space Agency (ESA).

[e]USSR-France.

[f]Main Belt Asteroid Rendezvous, Near Earth Asteroid Rendezvous, Saturn Flyby-Saturn Probe.

[g]Goldstone Solar System Radar, host-country radio astronomy.

[h]Search for Extraterrestrial Intelligence.

Table 2. Definitions of Ka-band options

Subnet	Services[a]	Configuration Options
34-meter standard (DSS-12 etc.)	S/SX[b] X/XKa (+S desired) C/C[c] Ku/Ku[c]	• Replace with center-fed beam waveguide antenna similar to new DSS-13 nucleus. • Replace with HEF-type antenna with multiband feedcone.
34-HEF subnet (DSS-15 etc.)	X/SX X/XKa	• Modify with multi-band feedcone. • Retrofit with bypass BWG and alidade feed room. • Rebuild for center-fed BWG into a feed room.
70-meter subnet	S/S S/SX X/SX X/XKa (+S desired) C/L[c] C/C[c] Host radio astronomy Radar astronomy (including megawatt)	• Tricone structure, modified as needed. • Monocone, possibly in 3 sectors. • Partial bypass BWG to carry new services in higher frequency bands, while leaving the S/S and S/SX high-performance elements in two legs of the current tricone. • Retrofit the existing antenna with a full bypass BWG providing all services. • Replace the existing antenna with a new 70-meter antenna similar in design to the Usuda-64.

[a] Services available in 1988 will continue to be needed through the period of interest with essentially no change in performance quality (effective isotropic radiated power and gain/temperature). Added services vary by subnet.

[b] Indicates concurrent uplinking at S-band and downlinking at S- and X-bands. Similar notation occurs throughout the table.

[c] Separable option.

Table 3. Technological and environmental elements affecting or affected by Ka-band

Element	Impacts
Ionosphere	Radio metric delay and stability
Troposphere	Attenuation, noise temperature, weather
Antenna	Surface: Panel adjustment: static versus dynamic Holography assumed Pointing: Angle tracking and blind pointing Acquisition process Configuration Stability/deformation
Microwave	Configuration Bandwidth Stability LNA type Array feed: interaction with pointing
Receiver	Down-conversion/frequency span Phase-lock dynamics Stability Bandwidth Acquisition process Configuration: depends on microwave Coherent detection efficiency Doppler extractor: type and performance
Metrics	Bandwidth Doppler precision/stability Media effects Δ-DOR[a] and phase calibrations
Science usage	Primarily metrics
Telemetry rates	Customer-driven
Uplink	Stability (X/Ka multiplication) Rates/bandwidth: customer-driven
Predicts	Increased precision Responsiveness assumed fixed otherwise
Operations	Short pass/data dump option
Calibration beacon	Need a high-earth orbit spacecraft beacon

[a]Delta-differential one-way range

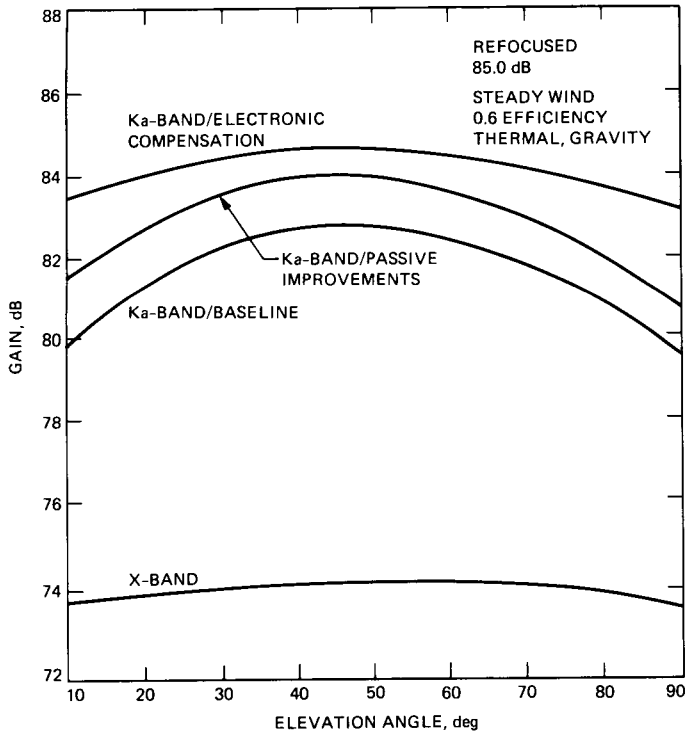


Fig. 1. 70-meter antenna performance at Ka-band.

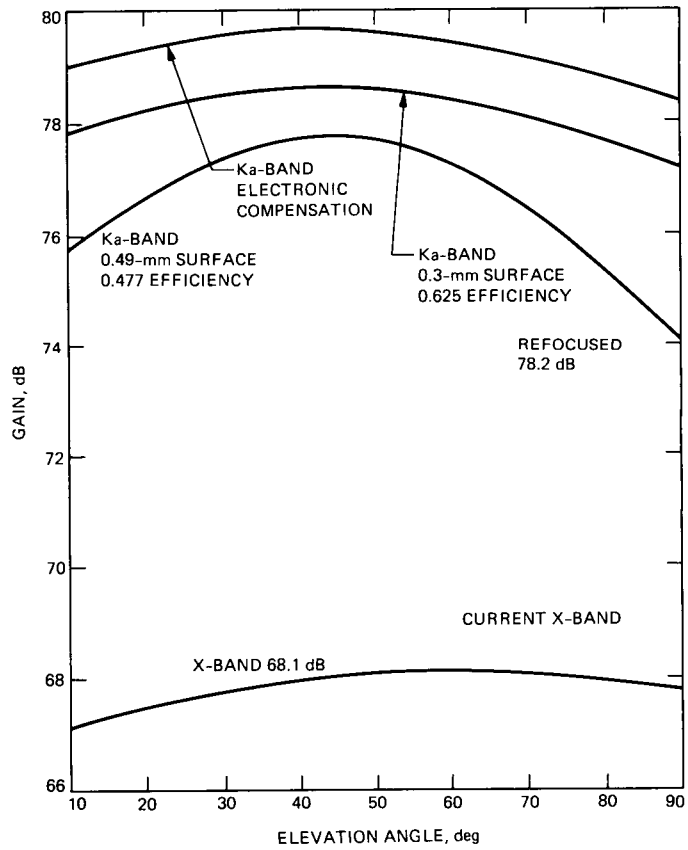


Fig. 2. 34-meter antenna performance at Ka-band.

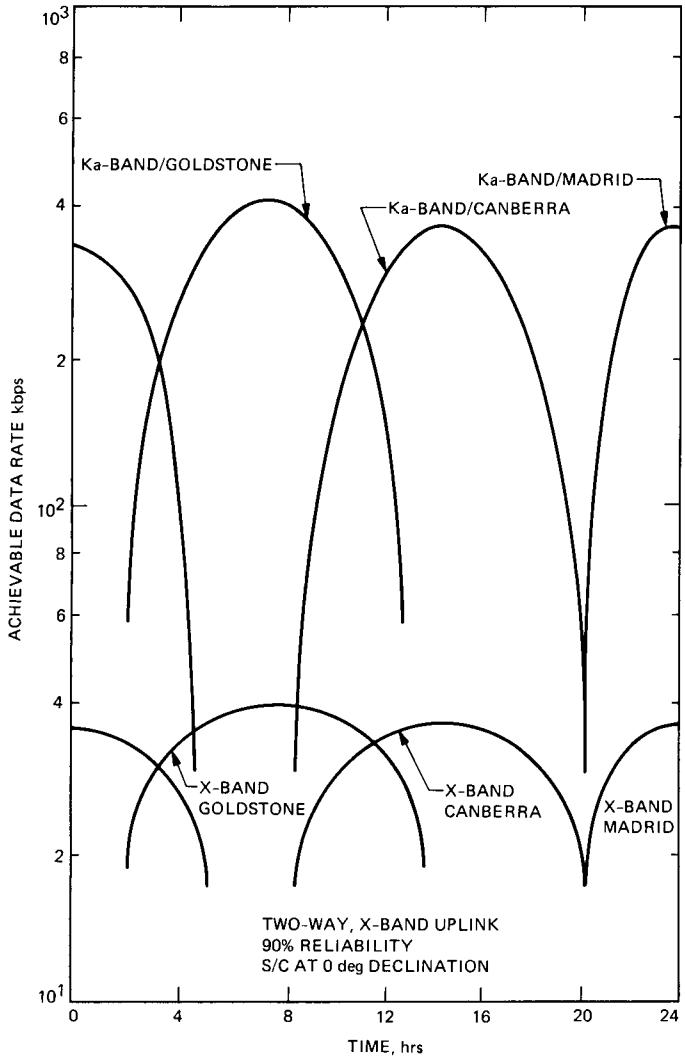


Fig. 3. Telecom performance advantage of Ka-band versus X-band.

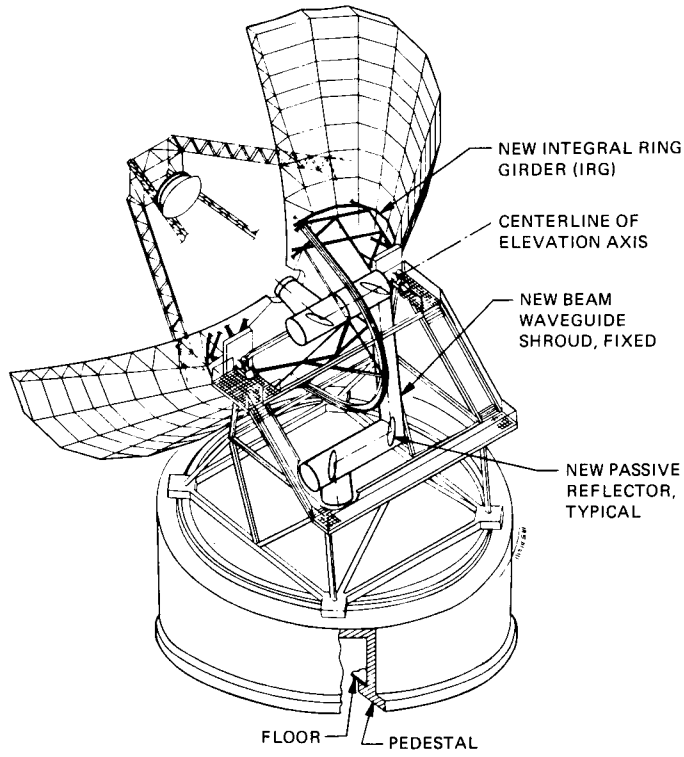


Fig. 4. Concept for new 34-meter replacement beam waveguide antenna.

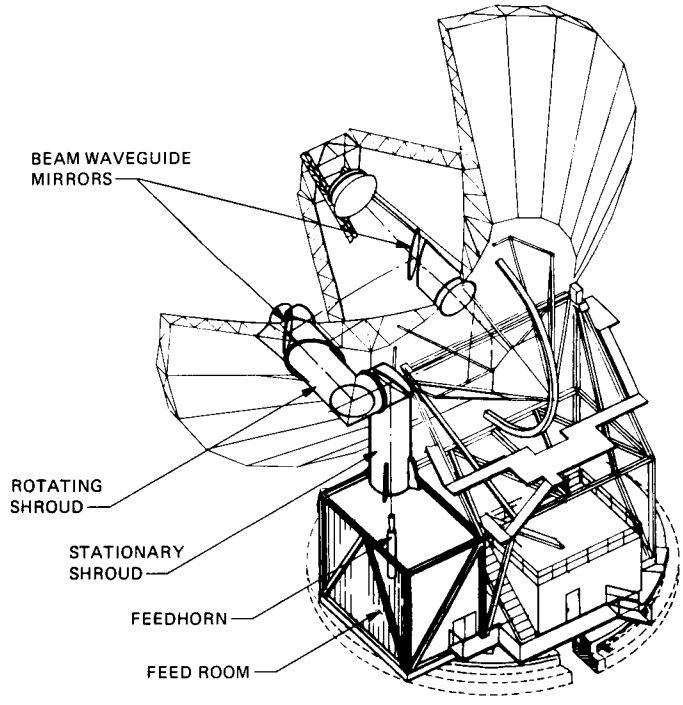


Fig. 5. Concept for modified 34-meter high-efficiency antenna with bypass beam waveguide.

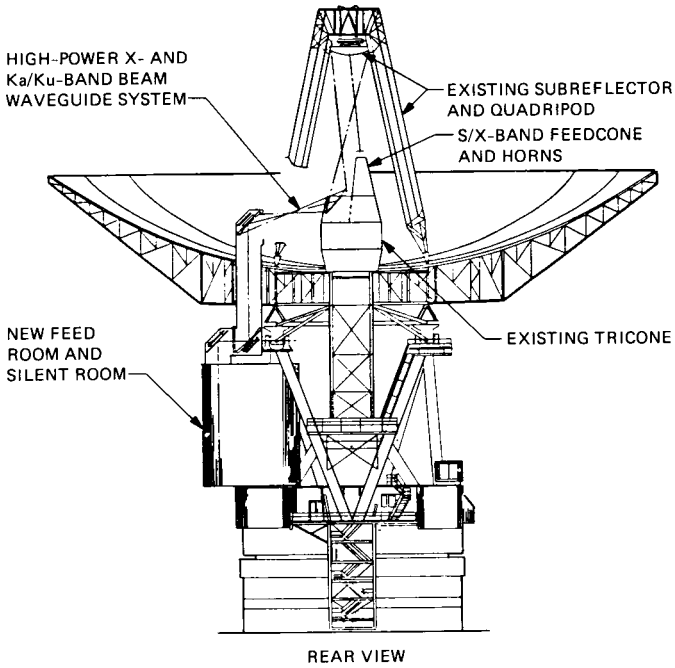


Fig. 6. Concept for 70-meter with hybrid beam waveguide.

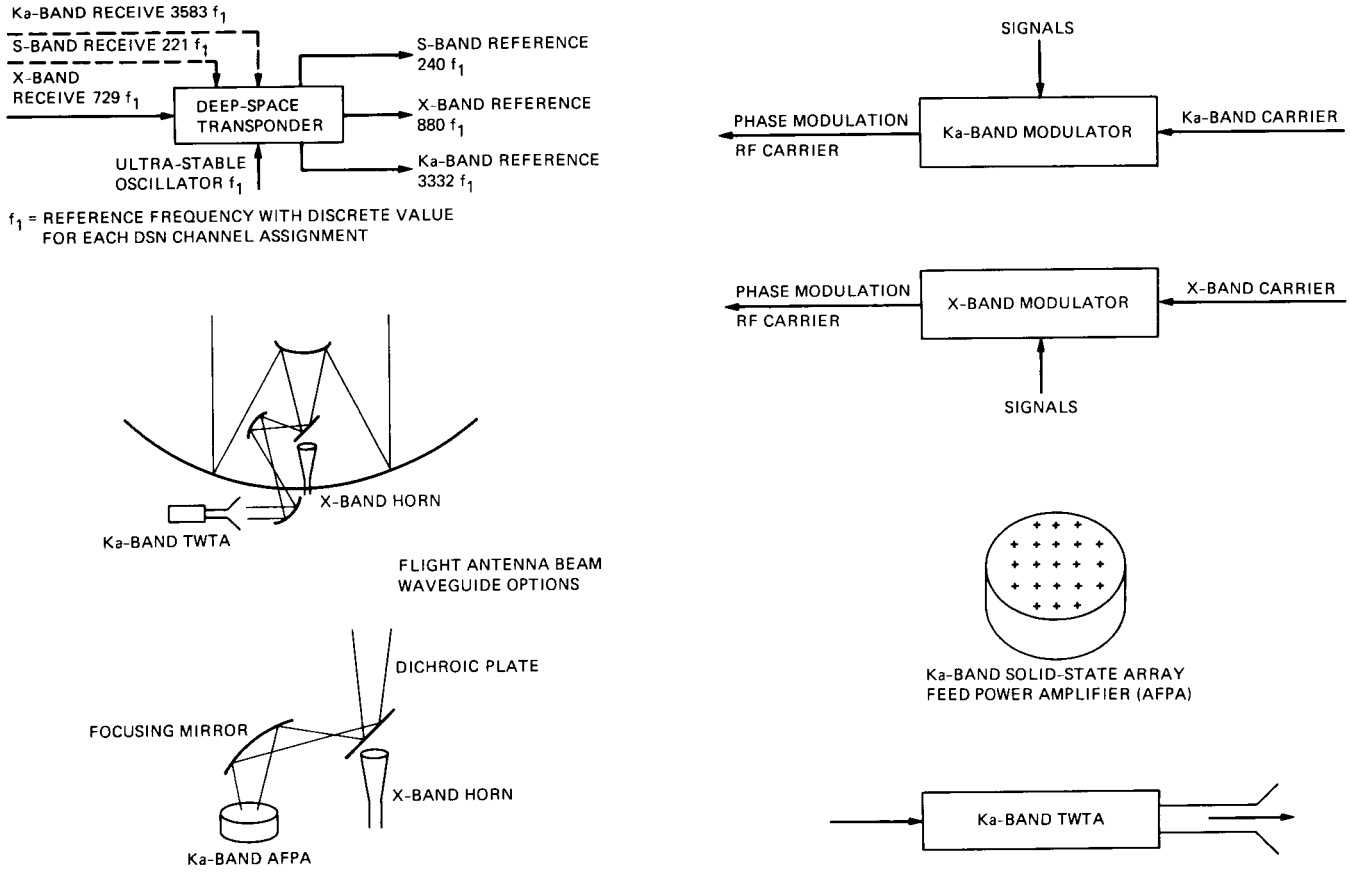


Fig. 7. Ka-band related spacecraft elements.

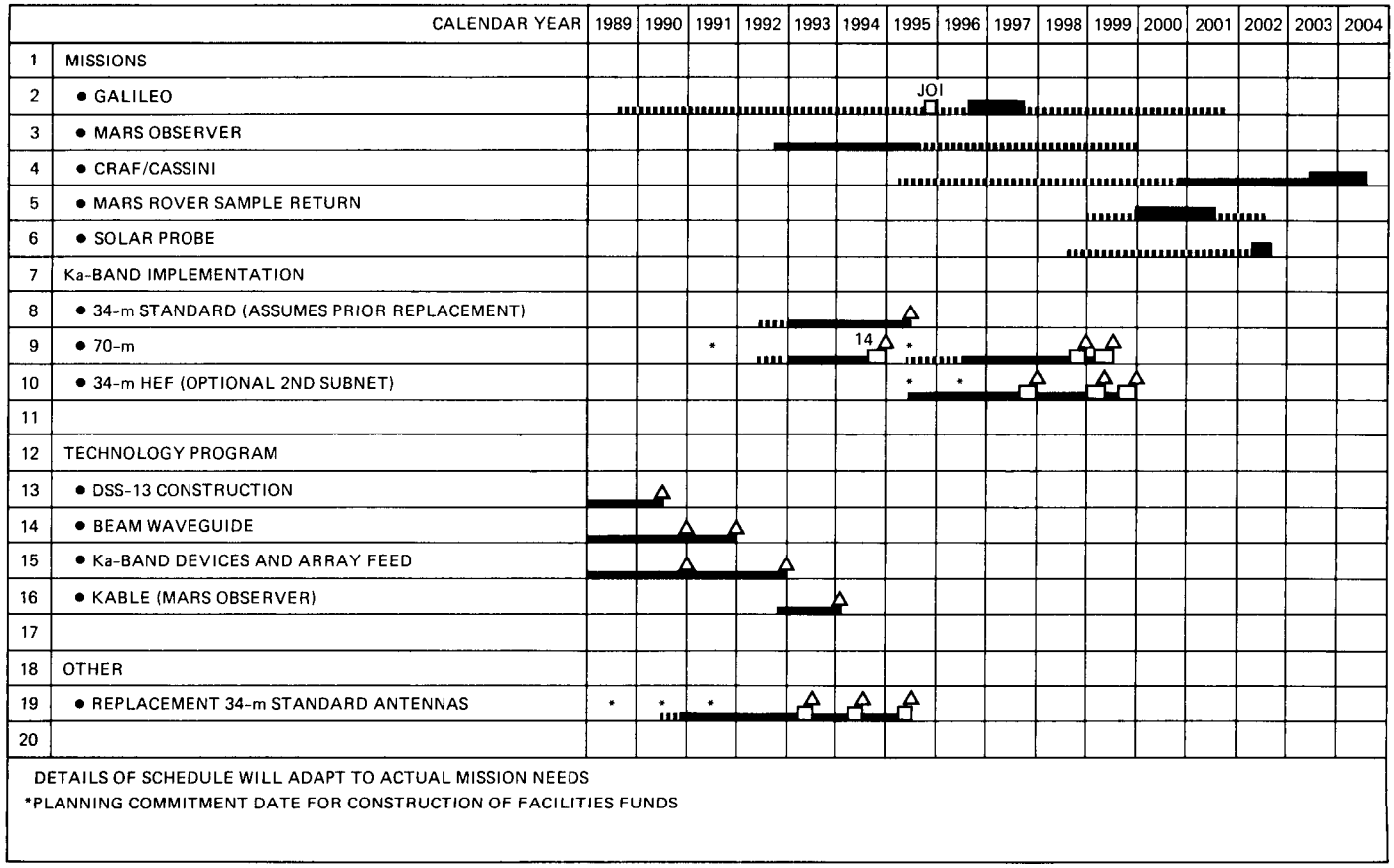


Fig. 8. Overview Ka-band schedule.

S14-33

P-7

TDA Progress Report 42-96 October – December 1988

193066

A Low-Loss Linear Analog Phase Modulator for 8415 MHz Transponder Application

N. Mysoor
Spacecraft Telecommunications Equipment Section

A breadboard single-section low-loss analog phase modulator with good thermal stability for a spacecraft transponder application has been analyzed, fabricated, and evaluated. A linear phase shift of 70 degrees with a linearity tolerance of ±7 percent was measured for this modulator from 8257 to 8634 MHz over the temperature range -20°C to 75°C. The measured insertion loss and the static delay variation with temperature were within 2 ±0.3 dB and 0.16 ps/°C, respectively. Four sections will be cascaded to provide the X-band (8415 MHz) phase modulator. The generic modulator design can also be utilized at 7950 to 8075 MHz followed by ×4 multiplication to provide modulation of a Ka-band downlink signal.

I. Introduction

A circulator-coupled reflection phase modulator has been analyzed and investigated to provide the capability to directly modulate an X-band (8415 MHz) downlink carrier for the next generation of spaceborne communications systems. The phase modulator must be capable of large linear phase deviation, low loss, and wideband operation with good thermal stability. In addition, the phase modulator and its driver circuit must be compact and consume low dc power. The design is to provide ±2.5 radians (±143 degrees) of peak phase deviation to accommodate downlink telemetry data and ranging. The tolerance on the phase deviation linearity is ±8 percent. The insertion loss should be less than 10 dB and its variation with phase shift should be within ±0.5 dB. The phase delay variation specifications over the transponder hardware qualification environment, -20 °C to 75 °C, are less than 32 ps/°C for the transponder, and less than 1 ps/°C for the phase modulator. Such stringent specifications make the hardware implementation rather difficult. This investigation will consider the reflection-type phase shifter for the implementation of the hardware. The results extrapolated from analyses and measured performance for a single-section phase modulator with high phase resolution capability are presented in this article. Theoretical analysis of the modulator is presented in Section II. The breadboard modulator configuration and test data are presented in Section III. The conclusions are presented in Section IV.

II. Phase Modulator Analysis

This investigation will consider the circulator-reflection-type phase shifter. A single-stage phase shifter is shown in Fig. 1. Theoretical analysis of the single-stage and multistage phase modulator circuits and their operational amplifier (op-amp) drive circuit are presented in the following subsections.

A. Analysis of a Single-Stage Reflection Phase Modulator

The varactor diode is well suited for the phase modulator application as it can provide rapid phase change with the applied voltage. The circuit model for a packaged diode terminating a transmission line of characteristic impedance Z_o for a reflective phase shifter is shown in Fig. 2. The junction capacitance of abrupt-junction silicon (Si) diodes is modeled as

$$\frac{C_j(V)}{C_o} = \left(1 + \frac{V}{0.8}\right)^{-n}$$

where $C_j(V)$ is the junction capacitance at reverse bias voltage V. C_o is the junction capacitance at $V = 0$.

The diode capacity variation parameter n is the slope of the capacitance-voltage (C-V) curve when plotted on a log-log scaled paper. This slope n is a function of the bias voltage and junction temperature. In the operating bias range of the diode, it can be treated as a constant. The diode capacity parameter n is equal to about 0.5 for practical abrupt-junction silicon diodes. For this analysis, an abrupt-junction silicon diode of capacitance C_j equal to 1 pF at −4 volts bias is considered. Shown in the circuit model of Fig. 2 are the diode junction capacitance, diode leakage resistance (R_s), package inductance (L_p), package capacitance (C_p), lead inductance (L_ℓ), parallel resistance (R_p), and 10-ohm transmission line. In order to obtain large linear phase shift, it is necessary to use a low-impedance transmission line at the diode terminal. The 10-ohm line was selected as it can be realized on a 10-mil-thick alumina substrate. In addition, its line width is not overly wide compared to its length and the diameter of the device package. The package parasitics and the line impedance are optimized to provide linear phase-shift variation with bias voltage. The selected values through analysis and optimization are R_s = 1.5 ohms, L_p = 0.19 nH, C_p = 0.085 pF, L_ℓ = 0.283 nH, and R_p = 100 ohms. The parallel resistance R_p at the diode plane is intentionally added to maintain the insertion loss constant. The calculated phase shift and insertion loss variations with the bias voltage for this model are shown in Fig. 3. The phase shift is linear over the 6- ±5-volt bias range. The linear phase shift over this range is ±65 degrees. The maximum deviation from linearity is within ±6 percent. Any deviation from the optimized circuit component values will result in a reduction in the linear phase-shift range. The circuit component values must be kept within ±10 percent of the optimized values for good results. In particular, the value of package parasitic inductance (L_p) must be within ±5 percent. The insertion loss variation over this voltage range is 2.2 ±0.1 dB. This insertion loss does not include the losses due to the circulator and transmission line matching sections. The estimated total loss including all losses for a single-stage phase shifter is about 3 ±0.1 dB. The insertion loss of a phase modulator must be kept constant with phase shift. The variation of the insertion loss with phase shift causes amplitude modulation (AM) of the RF signal. This AM may get converted to undesirable phase modulation (PM) by subsequent nonlinear operation. The insertion loss can be leveled over the phase-shift range by adding a stabilizing resistor (R_p) in parallel with the varactor diode of each stage (Fig. 2).

B. Analysis of Multistage Reflection Phase Modulator

A series cascade of three circulator-reflection phase shifters will provide ±200 degrees phase shift with ±6 percent error. The estimated total insertion loss, including the input and output isolators, is 10 dB ±0.5 dB. These predictions are based on the analysis of the single stage in the previous section. However, the measured data on the fabricated single-stage reflection phase modulators in Section III projects the use of four stages instead of three stages to meet the linearity requirement. A four-stage circulator-reflection phase modulator, including the modulator drive circuit, is shown in Fig. 4.

C. Phase Modulator Op-Amp Drive Circuit

The functions of the phase modulator drive circuit (Fig. 4) are to sum and amplify the modulation input signals and provide composite drive voltage to the varactor diodes. The modulation input signals include the spacecraft telemetry, ranging, and differential one-way ranging (DOR) signals. The modulation frequency range is from dc to 20 MHz. The selected wideband op-amp for this application is the Comlinear CLC 231. The estimated power dissipation for the drive circuit is 1 watt.

III. Phase Modulator Implementation and Performance

The circuit configuration and measured performance of the breadboard single-stage circulator-reflection phase modulator are given in subsection III-A. Application to Ka-band (31.8 to 32.3 GHz) is also presented in this subsection. The estimated projections for a four-stage phase modulator are presented in subsection III-B.

A. Single-Stage Circulator-Reflection Phase Modulator

1. Circuit Configuration. The circuit diagram and a photograph of the phase modulator are shown in Figs. 1 and 5, respectively. The reflection phase shifter configuration [1, 2] makes use of a 50-ohm circulator to provide matched input and output terminals for the phase-shifting diode circuit in the middle path. The circulator used in this investigation is a

broadband 8.4 to 12 GHz circulator (Western Microwave, Inc., 13CX-481, Serial no. 10). The two-way insertion loss of the circulator is 0.6 ±0.1 dB over the operating bandwidth at the nominal temperature of 23 °C. The circuit [Fig. 1] consists of a packaged diode at the end of a 10-ohm line and two quarter-wave matching sections (33.44-ohm and 14.95-ohm sections) to transform 10 ohms at the diode terminals to 50 ohms at the circulator port. The 10-ohm microstrip circuit is etched on a 10-mil-thick Roger 1085 substrate of dielectric constant K = 10.5. The width of the 10-ohm line is 97 mils, which is slightly larger (20 percent) than the diode package diameter of 80 mils. Better than 75 percent size matching between the diode and the line width is necessary in hybrid circuits to reduce insertion loss. The diode's anode is soldered to the ground as shown in Fig. 5. The circuit model for the diode, diode package parasitics, and connecting lead inductance are illustrated in Fig. 2. The junction capacitance of the selected abrupt-junction silicon diode (Alpha Industries, DVH 6733-02 in 168-001 package) is approximately equal to 0.6 pF at −4 volts bias, 0.45 pF at −8 volts bias, and 1.392 pF at 0 volts bias. This results in a diode capacitance ratio of 3:1 from from 0 volts to -8 volts bias range. Such large capacitance variation with bias is necessary to obtain large phase deviation. The series resistance of the diode is 3.6 ohms. The phase deviation characteristics of the circuit are also influenced by the values of package parasitics, interconnection lead inductance, and the length of the 10-ohm line. The typical values of the diode package parasitics supplied by the manufacturer are L_p = 0.5 nH and C_p = 0.18 pF. The inductance of the interconnection lead (L_ℓ) between the diode package and the 10-ohm line is equal to 0.05 nH. It is difficult to accurately model the package parasitics. The lengths of the interconnection lead (L_ℓ) and the 10-ohm line can be adjusted to obtain linear phase deviation.

2. Performance of Single-Stage Phase Modulator at 8415 MHz. The measured phase deviation versus bias characteristics for the single-section phase modulator (Fig. 5) are illustrated in Fig. 6. The nominal values of frequency, bias, voltage, and temperature in these measurements are 8415 MHz, 4.5 volts and 23 °C, respectively. The measurement bandwidth range was from 8257 to 8634 MHz. The phase angle was measured at 0 volts bias and the nominal frequency 8415 MHz was used as the reference angle. The measured linear phase deviation for the voltage swing ±3 volts above the nominal bias of 4.5 volts was ±34 degrees with a linearity better than ±7 percent of a best-fitted straight line (BSL). The phase modulator circuit was subjected to temperature tests over the hardware qualification temperature range from -20 °C to 75 °C. As shown in Fig. 7, the overall variation of the static phase with temperature is about 45 degrees with 0.5 degree/°C slope. The calculated static phase delay at 8415 MHz is 0.16 ps/°C. As seen from Fig. 7, the change in the static phase with temperature is not symmetrical about its value at 23 °C. The reason is that the static phase variation of the circulator with temperature is nonlinear. The measured value of the circulator's static phase shift was 2.2 degrees for a change in temperature from 23 °C to 75 °C, and was equal to -17.3 degrees from 23 °C to -20 °C. However, the temperature-induced phase shift for the diode circuit has a linear slope equal to 0.26 degree/°C. Measured insertion loss as a function of varactor bias and temperature are shown in Fig. 8. The RF input power level was equal to 5 dBm at 8415 MHz. The maximum variation of the insertion loss with circulator was found to be 2 ±0.3 dB over the bias levels (4.5 ±3 volts), temperature range (-20 °C to 75 °C), and the RF frequency range (8257 to 8634 MHz). This includes the circulator's two-way insertion loss of 0.6 dB. The diode phase shift and linearity can be calculated if all the circuit component values are known fairly accurately. The values of package parasitics and the diode's junction dynamics are not well known. This results in a discrepancy between the measured and predicted results.

3. Performance of Single-Stage Phase Modulator at 7966 MHz for Ka-Band (31.8 to 32.3 GHz) Application. The single-stage modulator was also evaluated at 7966 MHz to assess its applicability to the Ka-band (31.8 to 32.3 GHz) exciter subsystem. For the Ka-band application, the phase-modulated carrier at 7950 to 8075 MHz is multiplied by four to obtain the signal at Ka-band frequency. The measured phase deviation and insertion loss values are shown in Figs. 9 and 10. The measured bandwidth range about 7966 MHz was from 7807 to 8118 MHz. Figure 9 shows a linear phase shift of ±36 degrees at 7966 MHz with a linearity of ±8 percent over the bias range of 4 volts ±3.5 volts. The insertion loss is flat and is equal to 2 ±0.3 dB. The full phase deviation of ±143 degrees at Ka-band (31.8 GHz) can be obtained by multiplying the output of the single-stage phase modulator (±36 degrees) at 7966 MHz by a ×4 multiplier. The circuit is thus useful for both 8415 MHz (X-band) and 7966 MHz applications (applicable to Ka-band at 4 × 7966 MHz). The measured overall bandwidth of this circuit is 2300 MHz, from 6900 to 9200 MHz.

B. Four-Stage Circulator-Reflection Phase Modulator

Four of the above-mentioned circulator-reflection phase shifter circuits (Fig. 4) in tandem will provide ±143 degrees of linear phase deviation at 8415 MHz, with linearity better than ±8 percent and insertion loss of about 10 ±0.5 dB. The bias range is 4.5 ±3 volts. The estimated size of the 8415 MHz four-stage phase modulator including the wideband op-amp drive circuit is 5.72 by 5.72 by 2.2 cm.

IV. Conclusions

Using a given package-type varactor diode and a circulator, a phase modulator was realized. From 8257 to 8634 MHz, the measured voltage-controlled linear phase deviation, linearity tolerance, and insertion loss were ±34 degrees, ±7 percent, and 2 ±0.3 dB, respectively, over the test temperature range of −20 °C to 75 °C. The static phase delay was found to be 0.16 ps/°C. It is feasible to construct a ±143 degree phase modulator using four such reflector phase-shifting circuits with approximately 10 ±0.5 dB of insertion loss.

Acknowledgments

Acknowledgment is given to the contributions of C. N. Byrom and A. W. Kermode during the course of this work.

References

[1] R. Garver, "360° Varactor Linear Phase Modulator," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 137–147, March 1969.

[2] R. Garver, "Broad-Band Diode Phase Shifters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 314–323, May 1972.

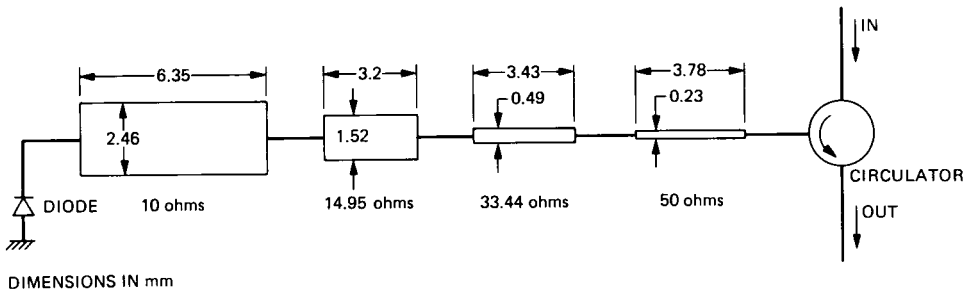


Fig. 1. Phase modulator circuit layout etched on a 0.254-mm-thick soft substrate of dielectric constant $K = 10.5$.

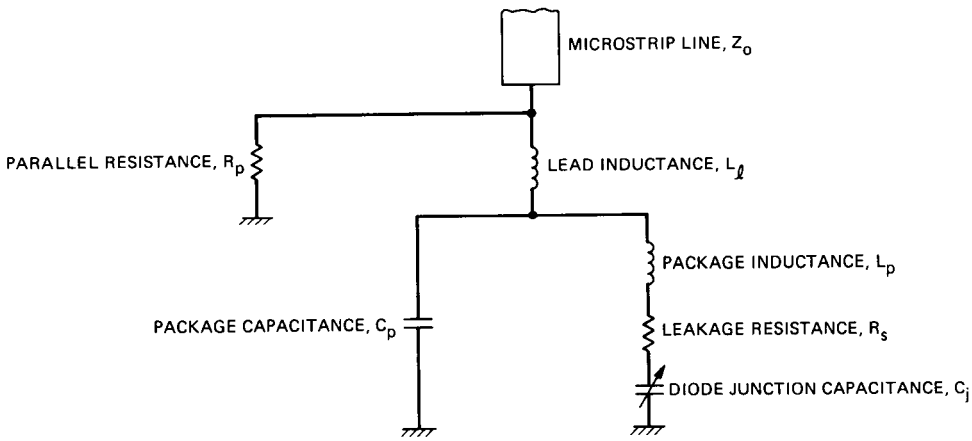


Fig. 2. Phase modulator circuit model.

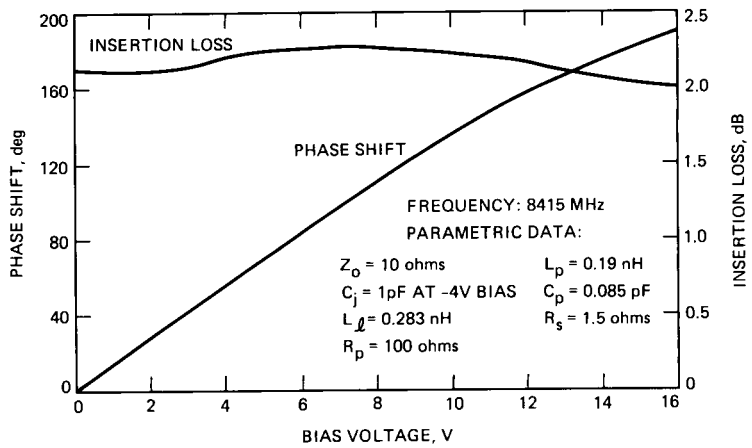
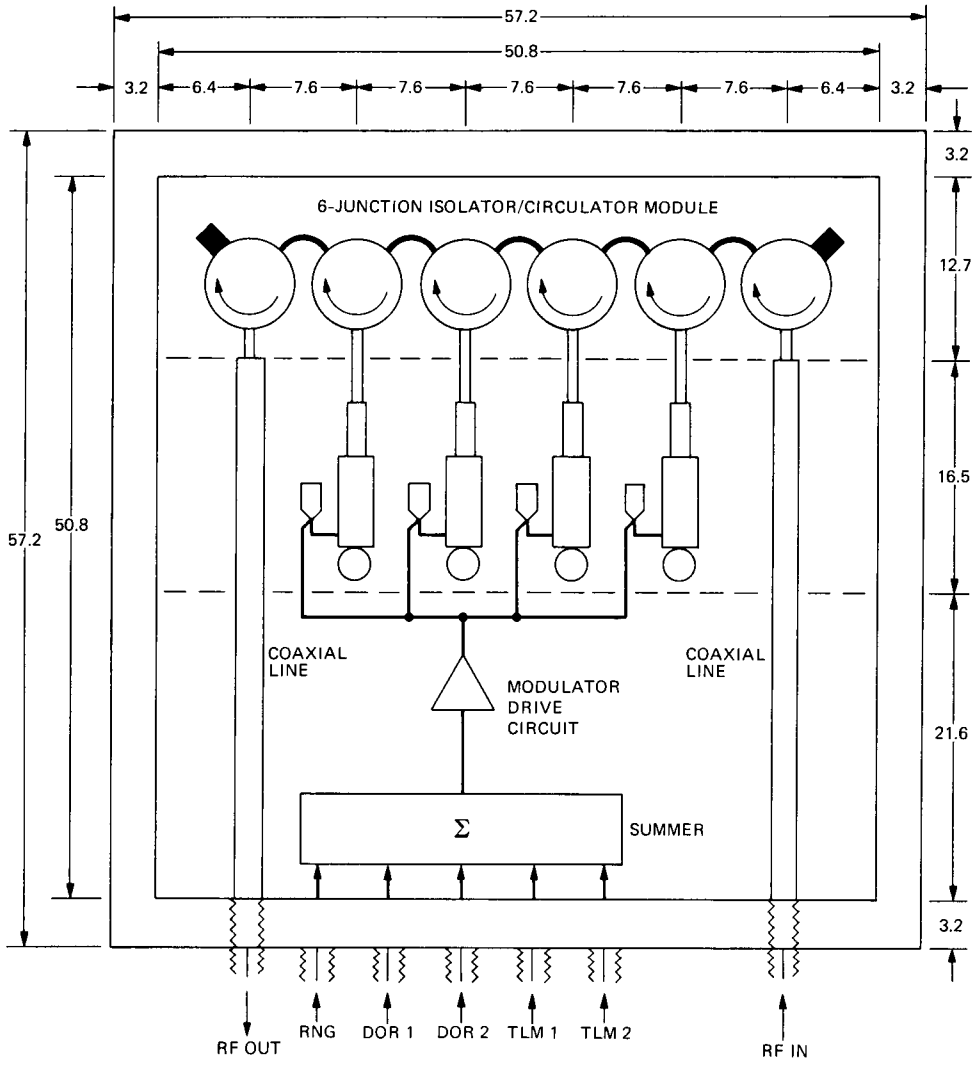


Fig. 3. Calculated phase shift of an optimized single-section phase modulator as a function of dc bias voltage.



OUTSIDE DIMENSIONS: 57.2 x 57.2 x 21.6
DIMENSIONS IN mm

Fig. 4. Four-stage circulator-reflection phase modulator.

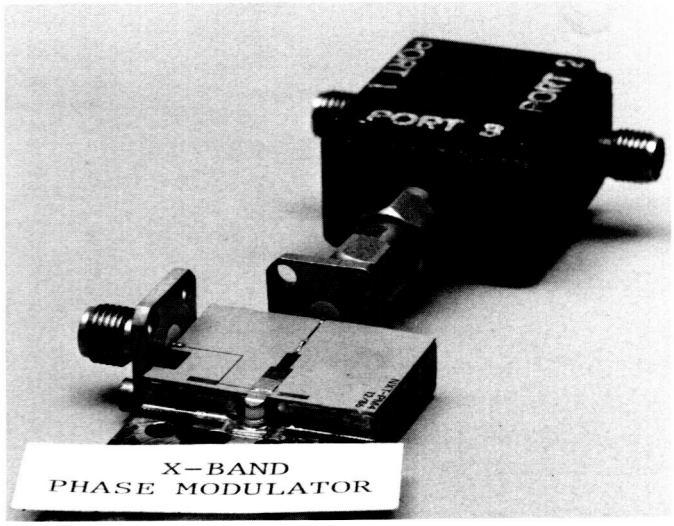


Fig. 5. X-band (8415 MHz) phase modulator.

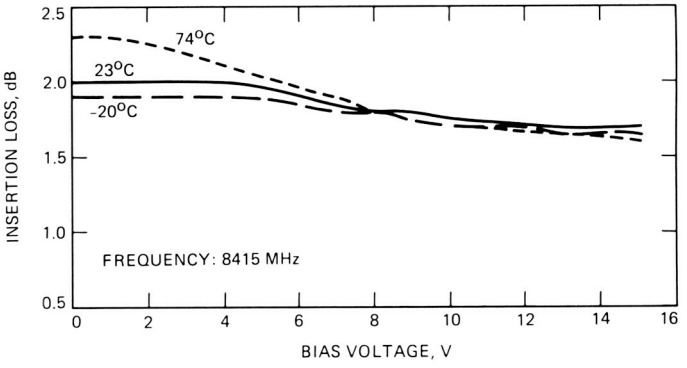


Fig. 8. Measured insertion loss versus dc bias voltage and temperature.

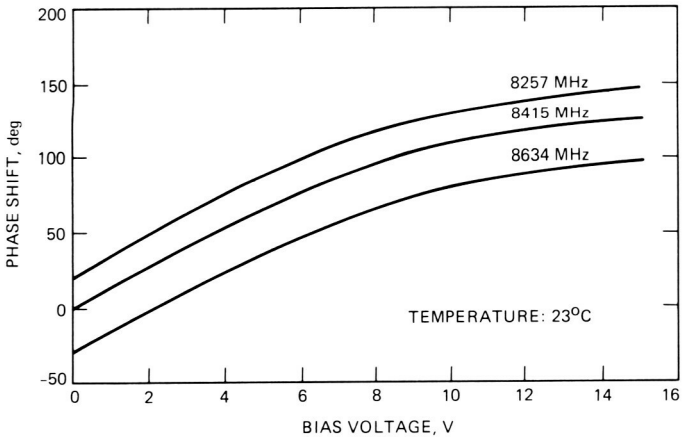


Fig. 6. Measured phase shift as a function of dc bias voltage and frequency.

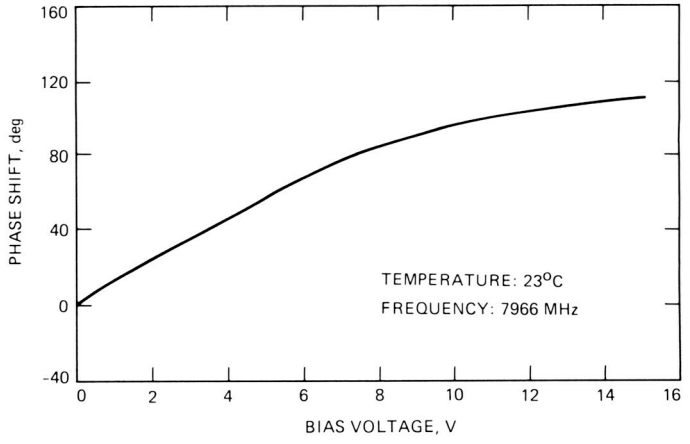


Fig. 9. Measured phase shift versus dc bias voltage.

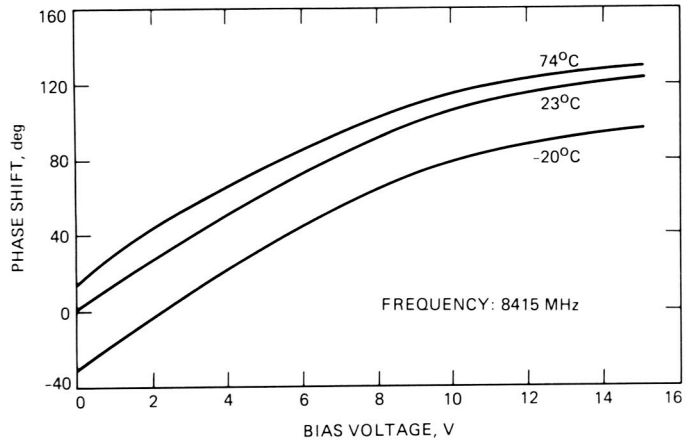


Fig. 7. Measured phase shift versus dc bias voltage and temperature.

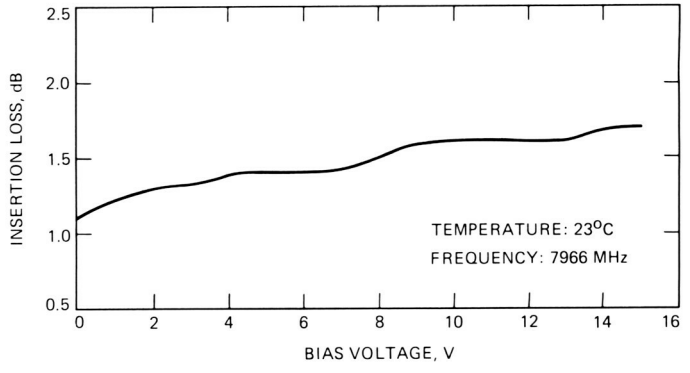


Fig. 10. Measured insertion loss versus dc bias voltage.

Radio Frequency Interference Survey Over the 1.0–10.4 GHz Frequency Range at the Goldstone-Venus Development Station

S. Gulkis and E. T. Olsen
Space Physics and Astrophysics Section
M. J. Klein and E. B. Jackson
Telecommunications and Data Acquisition Science Office

The results of a low sensitivity Radio Frequency Interference (RFI) survey carried out at the Venus Station of the Goldstone Communications Complex are reported. The data cover the spectral range from 1 GHz to 10.4 GHz with a 10-kHz instantaneous bandwidth. Frequency and power levels were observed using a sweep-frequency spectrum analyzer connected to a 1-m diameter antenna pointed at zenith. The survey was conducted from February 16, 1987 through February 24, 1987.

I. Introduction

Plans are currently being made at the Jet Propulsion Laboratory to carry out a comprehensive, all-sky search for radio signals of extraterrestrial origin. The Search for Extraterrestrial Intelligence (SETI) survey will employ the Goldstone Communication Complex near Barstow, California and other sites in the northern and southern hemispheres. The principal parameters of this survey are given in Table 1. In preparation for this search, JPL has constructed a radio spectrum surveillance system (RSSS) and made a series of measurements of the RFI environment at the Goldstone-Venus development station. Described in this article are the receiving system used [1], and the results of one low-sensitivity survey performed February 16-24, 1987. Additional surveys in restricted frequency bands and with higher sensitivity have been carried out in the interim. These surveys have not been fully analyzed at this time. This RFI survey effort is expected to continue for several more years. Efforts will be concentrated on establishing trends and on attaining sensitivity commensurate with levels that will be achieved by SETI.

II. The Radio Spectrum Surveillance System

The RSSS used for the observations reported here consisted of a log-periodic feed, a 1-meter parabolic antenna, a set of seven GaAs FET amplifiers (followed by transistor amplifiers) covering the spectrum from 1.0–10.4 GHz, and a Tektronix 494P swept spectrum analyzer. Figure 1 shows a block diagram of the receiving system. A Tektronix 4052A digital computer/controller automatically controls the antenna azimuth, noise diode, amplifier section, spectrum analyzer, and dual-floppy disk recorder. The spectral data are processed in the 4052A in near real time to determine whether a specified power threshold has been exceeded anywhere in the

spectrum. The data describing such events are written on the floppy disks at the field station for further off-line analysis at JPL.

The antenna and amplifiers are mounted atop the roof of a mobile trailer van. The spectrum analyzer, computer, and recording equipment are mounted in a rack inside the van. For the observations reported here, the van was parked at the Goldstone-Venus development station (DSS 13), about 30 meters south-west of the main control building. In this location, the van is approximately 150 meters east of the 26-meter antenna. Figure 2 shows a photograph of the site to illustrate the relative positions of the control building, the 26-meter antenna, and the RSSS.

Data recorded on the floppy disks are taken to JPL and copied onto a hard disk of a VAX 11/750 computer for further analysis. A commercially available database program, INGRES, is used to retrieve the data; custom software is used in conjunction with INGRES to perform parameter searches and generate various graphical displays.

III. Observations

The observations were carried out in a fully automated mode by pre-scheduling the controller to scan the spectrum analyzer from 1.0 GHz to 10.4 GHz repeatedly at a resolution bandwidth of 10 kHz. The time required to complete a single-frequency scan was 40 minutes, and in total, 232 scans were made over the course of the survey. In order to expedite the survey, the antenna main beam remained motionless and pointed in the direction of the zenith instead of scanning the horizon. In the zenith orientation, the antenna gain resembles that of an omnidirectional antenna for radiation that arrives along the horizon. Assuming that the antenna gain in the direction of the horizon is the same as that from an omnidirectional antenna, the effective area for the survey is approximately $0.1 \times \lambda^2$, where λ is the wavelength of the observation. The effective area for on-axis signals is approximately 0.5 m^2. Power levels reported in this article assume an omnidirectional antenna.

Each frequency was observed a total of 232 times, with nearly uniform coverage with time of day. Figure 3 shows the distribution of observations ("looks") with day of the week. Each day of the week is further divided into six 4-hour intervals starting at midnight. The weekdays Monday and Tuesday were observed most frequently because the survey began on a Monday and extended for nearly nine contiguous days. Sunday was observed least frequently because of an interruption due to a full storage disk. Only the first 4-hour interval (midnight to 4:00 a.m.) was observed on Sunday. A system noise temperature calibration was automatically performed daily between 3:00 a.m. and 4:00 a.m. local time. Table 2 gives the parameters used in the survey.

IV. Results

A total of 37,589 events were detected in the survey. Figure 4 shows a histogram of the number of events exceeding the threshold as a function of received power level. Note that the power levels for some interfering signals exceeded –90 dBm. These signals were traceable to local microwave transmitters. The relatively low number of signals detected with power levels less than –118 dBm is believed to be caused by the nonuniform sensitivity of the survey which varied by approximately 7 dBm from one end of the band to the other due to increasing receiver noise temperature at higher frequencies. It has not been concluded that weaker signals are less prevalent than stronger signals; further work is planned to clarify the situation at lower power levels. Figure 5 shows the cumulative distribution of events as a function of minimum received power level.

Figure 6 shows the probability of a signal exceeding the threshold as a function of frequency over the full frequency range of the survey, 1.0–10.4 GHz. The frequency resolution of the graph is approximately 10 MHz. This figure reveals that the probability is very nonuniform across the survey frequency range. The highest incidence of interference is in two frequency ranges: 1.0–3.0 GHz and 7.7–8.3 GHz. Figure 7 shows an enlargement of Fig. 6 in the frequency range 1.0–2.0 GHz. The frequency resolution of Fig. 7 is approximately 1 MHz. It can be seen from this figure that the "Water Hole" frequency range, 1.4–1.7 GHz, contains a significant amount of interference, but that the radio astronomy bands near 1.4 GHz and 1.6 GHz are relatively quiet, at least at the sensitivity achieved by this particular survey.

Figure 8 displays the probability of RFI events over the full 1.0–10.4 GHz range as a function of day of week. As in Fig. 3, each day is divided into six 4-hour intervals. Note that no observations were made between 0400 UT Sunday and 0400 UT Monday, which explains the lack of events during this time interval. This figure illustrates the pervasive nature of the interference. RFI events were observed every day of the week, with little change in probability of occurrence with time of day.

Table 3 provides a list of the frequencies and approximate frequency ranges that have exhibited an interfering signal at least 10 percent of the time they were observed. A worst-case estimate of the fraction of the observed band which is obscured by RFI can be made by adding up all the frequency ranges in Table 3. From this crude summation, it is found that 7.21 MHz, or approximately 7.7 percent of the 9.4-GHz survey bandwidth is affected by RFI at least 10 percent of the time.

A more detailed analysis of the raw data, examining each channel individually rather than in the frequency ranges indicated in Table 3, is shown in Fig. 9. This figure depicts the percent of the observed band obscured by RFI at least 10 percent of the time as a function of a limiting received power. The solid curve spanning the range from -100 dBm to -116 dBm is derived from the survey. Since the sensitivity level at which SETI will be operating is close to -170 dBm, it is of great interest to determine experimentally the shape of this curve at lower power levels. The dashed curves shown in Fig. 9 are crude extrapolations to lower power levels.

Several statistical models which might be helpful in providing a basis for understanding the present and future RFI survey results were considered. In the first model it was assumed that the effective isotropic radiated power (EIRP) of each transmitter is identical, that the transmitters are randomly distributed in area, and that the transmitter frequencies are randomly distributed. These assumptions are certainly incorrect since (1) transmitter frequency allocations are not random, (2) transmitter positions are generally clustered, and (3) EIRPs are not constant. Nevertheless, the model describes the extreme situation of extrapolating the local environment at Goldstone to more distant regions, assuming the areal density of transmitters is constant. For this model, the fraction of the survey band obscured, f, as a function of the received power, P, is given by the expression:

$$f = 1 - e^{-\frac{k}{P}} \tag{1}$$

where k is a constant. The constant, k, is a function of the areal density of transmitters, the fractional bandwidth covered by each transmitter, the EIRP of each transmitter, and the collection area of the receiving system. The dashed curve in Fig. 9 shows a graph of this equation with k taken to be -136.7 dBm (note: convert power from dBm to Watts when using the equation). This equation thus predicts that 63 percent of the band is obscured at the -136.7-dBm level. Preliminary results of a subsequent survey, not reported here, show that the interference is much less than this model predicts. The spatial distribution could just as well have been ignored in this model, and the spectral power density assumed to arrive at the same result. In reality, some combination of areal density and spectral power distribution are needed for a complete description.

A simple estimate of a lower bound for this model can be made by assuming that the areal density of transmitters goes abruptly to zero at some arbitrary radius. This condition might exist if the detectable transmitters were clustered near Goldstone, or if distant transmitters were obscured by the horizon. This lower bound model can be expressed by the pair of equations:

$$\begin{aligned} f &= 1 - e^{-\frac{k}{P}} \qquad P \geqslant P_m \\ f &= 1 - e^{-\frac{k}{P_m}} \qquad P \leqslant P_m \end{aligned} \tag{2}$$

The locus of points defined by these equations is shown by the two dotted lines in Fig. 9. Each assumes the same value of k as above but different minimum power cutoffs. One is drawn for a value of P_m = -125 dBm, and the other for a value of P_m = -114 dBm.

It is impossible to draw any firm conclusions about these models until more sensitive survey data are available. The models are highly simplified and do not consider the reality of more than one population of transmitters. For example, the sensitivity of this survey was too low to detect signals from geosynchronous satellites. We emphasize that any attempt to extrapolate these data to the power levels of interest to SETI is considered to be highly uncertain because of the more than 50-dBm power level difference between the experimental data and the SETI power regime.

V. Conclusions

It is concluded from this low-sensitivity, broad-band survey that most of the strong (> -116 dBm) RFI in the 1-10 GHz band occurs in relatively few bands. Nearly 1 percent of the entire band shows interference at the -116-dBm level or stronger with a probability of occurrence ⩾10 percent. The interfering signals do not appear to show a strong dependence on time of day or on day of the week. Interfering signals from satellites will probably show up at power levels significantly less than were achieved in this survey. Surveys at approximately 30 dB better sensitivity can be achieved with the current RSSS in a reasonable time through (1) use of a discone antenna to provide higher sensitivity along the horizon, and (2) observing with a more narrow bandwidth. Observations are currently being made with higher sensitivity using both of these techniques. Surveys at even greater sensitivity, approaching those achieved by SETI in the sidelobes, must await more sensitive systems.

Reference

[1] B. Crow, A. Lokshin, M. Marina, and L. Ching, "SETI Radio Surveillance System," *TDA Progress Report 42-82*, vol. April–June 1985, Jet Propulsion Laboratory, Pasadena, California, pp. 173–184, August 15, 1985.

Table 1. All-sky survey parameters

Spatial coverage	Entire celestial sphere
Frequency range	1–10 GHz inclusive and higher frequency spot bands
Duration	≈ 6 years
Frequency resolution	≈ 30 Hz
Instantaneous bandpass	≈ 250 MHz
Sensitivity	$\leq 10^{-23}\sqrt{\upsilon_{GHz}}\ Wm^{-2}$
Polarization	Simultaneous dual circular
Signals	Primarily CW with natural radio astronomy fallout

Table 2. Survey 1 parameters

Start date	February 16, 1987
Stop date	February 24, 1987
Number of sweeps	232
Antenna orientation	zenith
Frequency range	1.0–10.4 GHz
Resolution	10 kHz
Time constant	5×10^{-4} sec
Baseline level	−133 dBm at 1 GHz, −126 dBm at 10 GHz
Threshold	10 dB above the baseline level

Table 3. Frequencies with probability of interference ≥ 10 percent

Center Frequency of RFI, MHz	Probability of RFI	RF Range Affected	Band Allocation[a]
1000.015	0.6	< 10 kHz wide	AN
1051.685	0.4	< 10 kHz wide	AN
1085.420	0.5	1085.4 MHz–1085.44 MHz	AN
1134.600	0.1	< 10 kHz wide	AN
1165.975	0.6	1165.94 MHz–1166.11 MHz	AN
1302.515	0.4	1302.5 MHz–1302.53 MHz	A
1310.850	1.0	< 10 kHz wide	AN
1723.410	0.2	< 10 kHz wide	F&M
1723.525	0.6	< 10 kHz wide	F&M
1723.640	0.2	< 10 kHz wide	F&M
1724.525	1.0	1724.5 MHz–1724.55 MHz	F&M
1905.020	0.6	< 10 kHz wide	F&M
2000.030	0.1	< 10 kHz wide	F&M
2110.850	0.1	< 10 kHz wide	AF&M
2112.420	0.2	< 10 kHz wide	F&M
2115.225	1.0	< 10 kHz wide	F&M
2605.020	0.5	< 10 kHz wide	BS
7786.785	0.9	7784.39 MHz–7789.18 MHz	F
7832.015	0.2	< 10 kHz wide	F
7879.970	0.5	7879.95 MHz–7879.99 MHz	F
7884.960	0.7	7884.93 MHz–7884.99 MHz	F
7889.970	0.3	7889.96 MHz–7889.98 MHz	F
7934.430	0.3	7934.15 MHz–7934.71 MHz	F&MS
7934.960	0.3	7934.89 MHz–7935.03 MHz	F&MS
7935.110	0.1	< 10 kHz wide	F&MS
7935.355	0.4	7935.25 MHz–7935.46 MHz	F&MS
7935.770	0.2	7935.69 MHz–7935.85 MHz	F&MS
8080.050	0.8	8079.73 MHz–8080.37 MHz	F&MS
8179.910	1.0	8179.88 MHz–8179.94 MHz	F&MS
8260.095	0.4	8260.06 MHz–8260.13 MHz	F&MS
8359.910	0.5	8359.89 MHz–8359.93 MHz	F&MS

[a]A = Aeronautical AN = Aeronautical Navigation BS = Broadcasting Satellite
F = Fixed F&M = Fixed & Mobile F&MS = Fixed & Mobile Satellite
(Partial listing from "Tables of Frequency Allocations and Other Extracts" from *Manual of Regulations and Procedures for Federal Radio Frequency Management*, Superintendent of Documents, Washington, D.C., January 1984.)

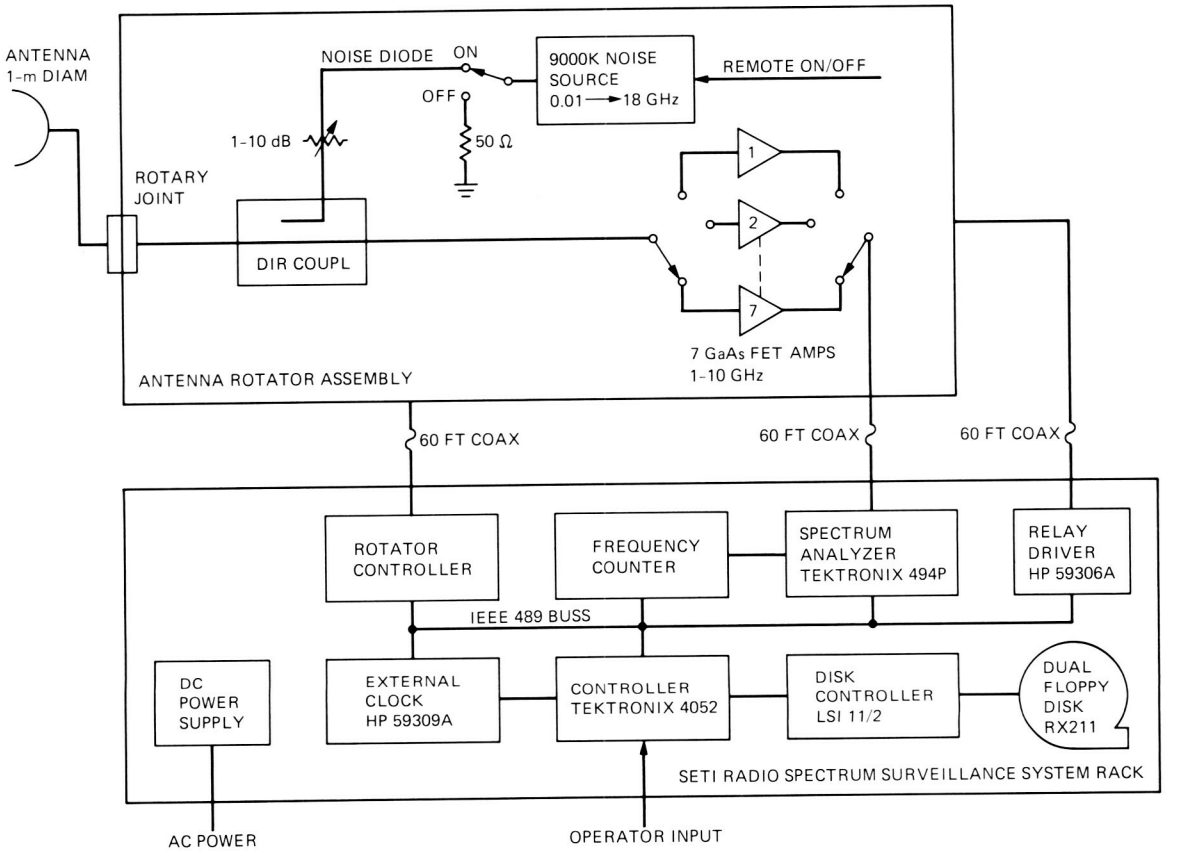


Fig. 1. Radio Spectrum Surveillance System (RSSS) block diagram.

Fig. 2. Photograph of RSSS mounted on mobile van at Goldstone-Venus development station.

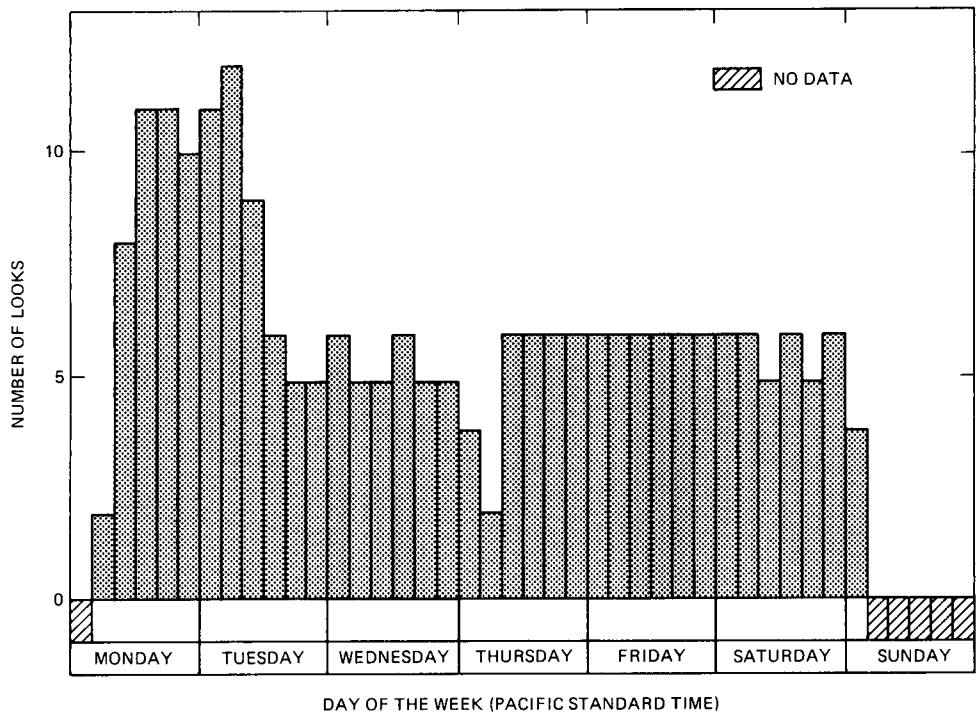


Fig. 3. Number of looks versus day of week for Survey 1, 1.0–10.4 GHz.

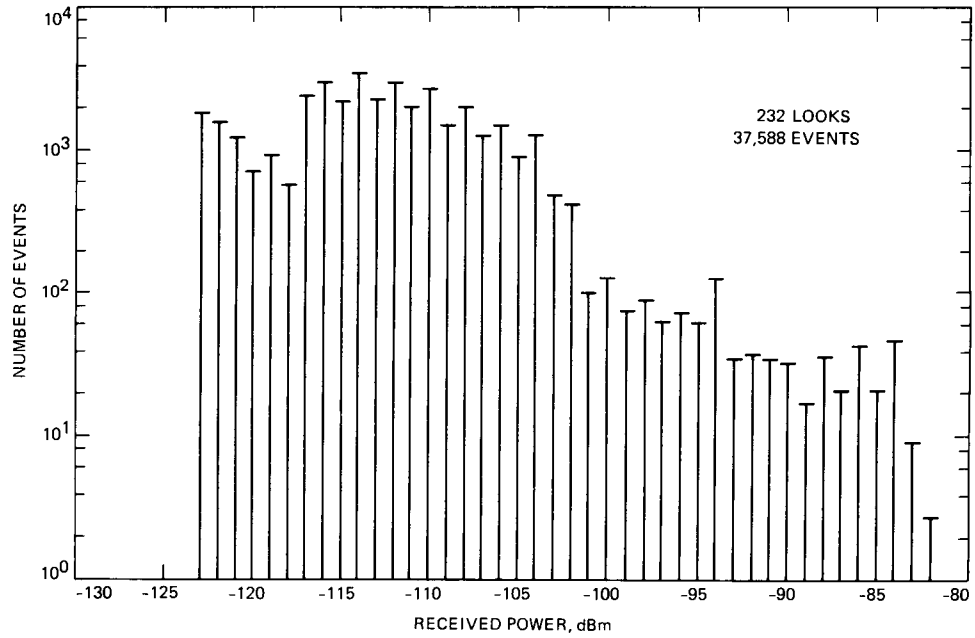


Fig. 4. Histogram of number of RFI events as a function of received power for Survey 1, 1.0–10.4 GHz.

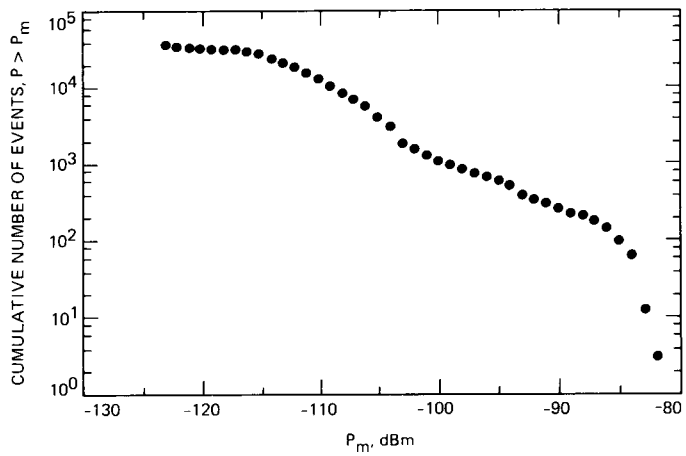


Fig. 5. Cumulative histogram of number of RFI events as a function of P_m for Survey 1, 1.0–10.4 GHz.

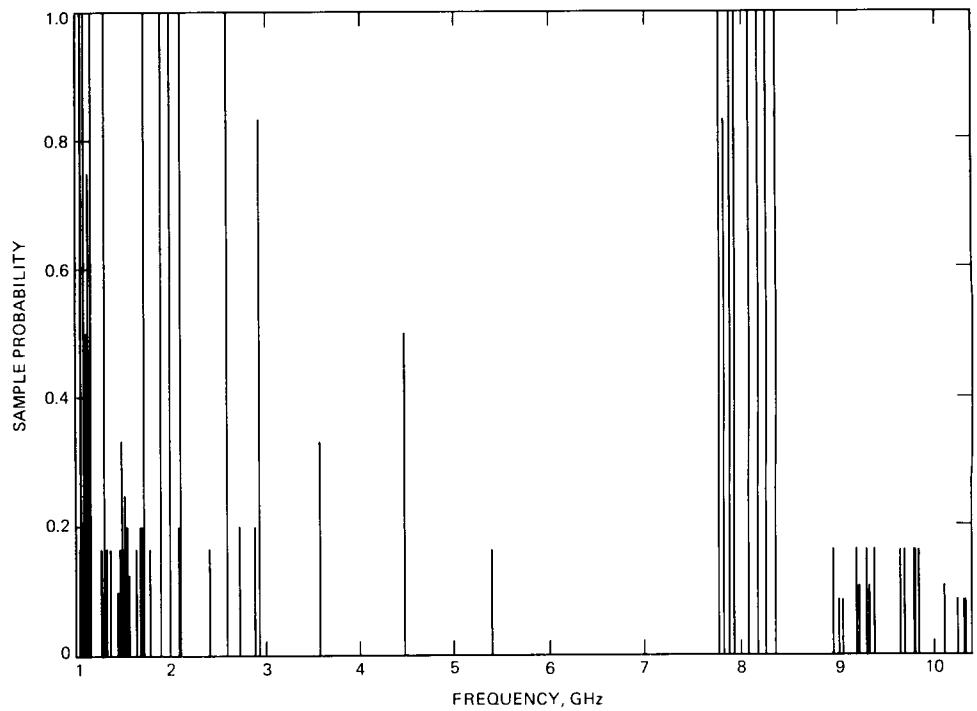


Fig. 6. Probability of RFI events as a function of frequency for Survey 1, 1.0–10.4 GHz.

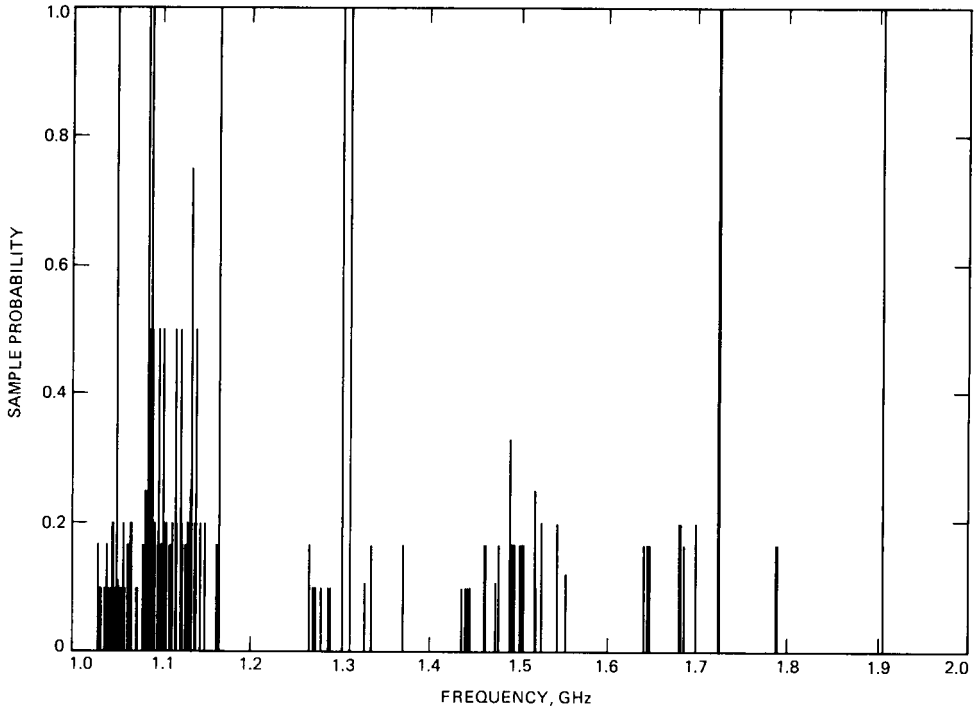


Fig. 7. Probability of RFI events as a function of frequency for Survey 1, 1.0–2.0 GHz.

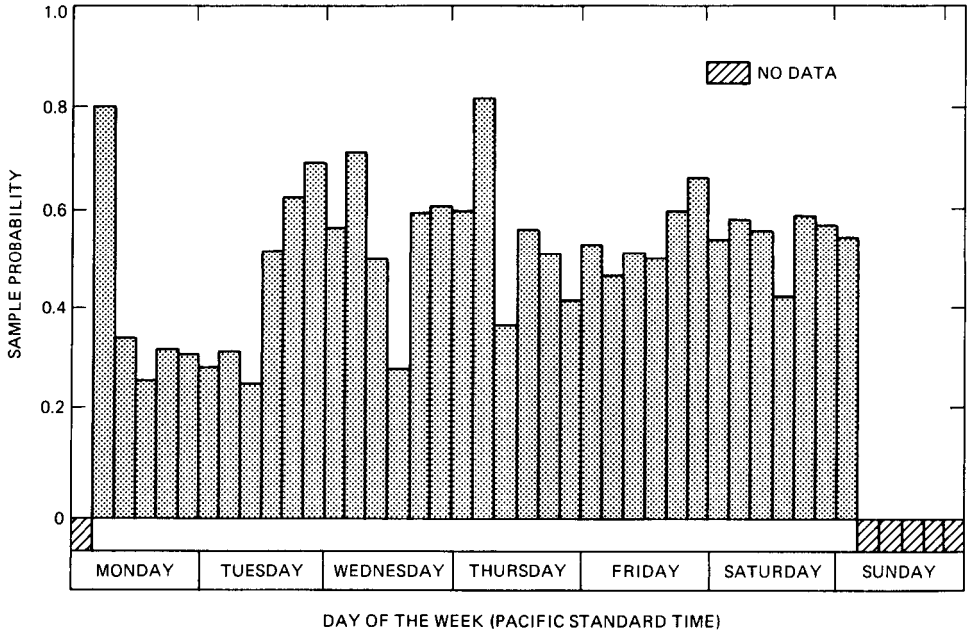


Fig. 8. Probability of RFI events as a function of 4-hour slice of day of week for Survey 1, 1.0–10.4 GHz.

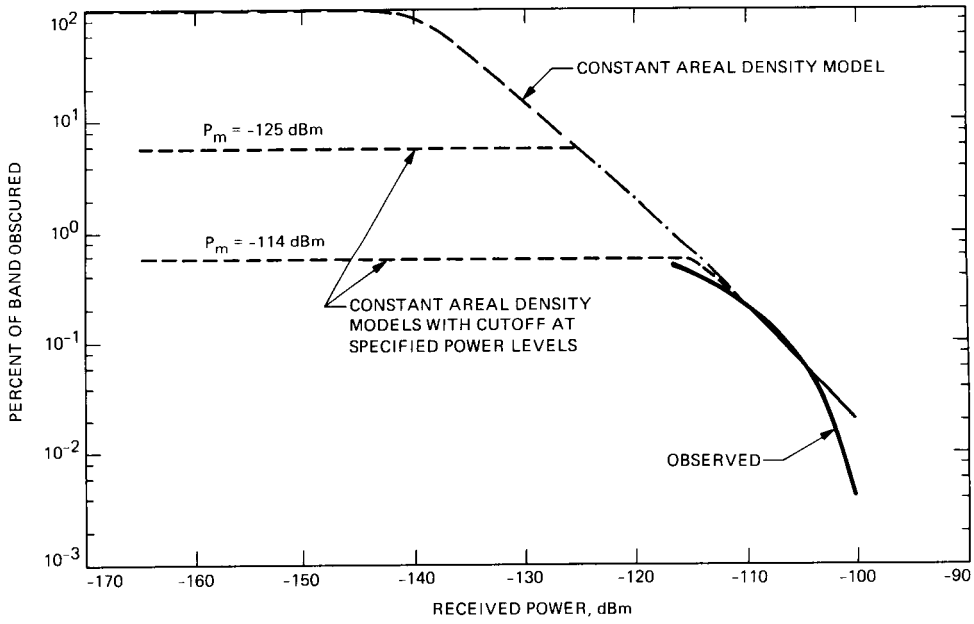


Fig. 9. Observed and extrapolated percent of bandpass obscured by RFI events with probability greater than 10 percent, 1.0–10.4 GHz.

Errata

R. E. Hill (Ground Antenna and Facilities Engineering Section) has submitted the following errata to his article "A New State Space Model for the NASA/JPL 70-Meter Antenna Servo Controls" that appeared in the *Telecommunications and Data Acquisition Progress Report 42-91*, July–September 1987, November 15, 1987:

In Table 2 (page 253), the denominator, J_i, appearing in the equation for $\dot{x}_2$ should be replaced with J_B. The variable, x_i, appearing in the equation for $\dot{x}_{2i+4}$ should be replaced with x_1. The inequality symbol ($\neq$) appearing in the equation for $\dot{x}_{2i+4}$ should be replaced by a plus symbol (+).

In Table 3 (page 254), dashed lines are added to the linear system matrix to show the respective rows and columns corresponding to the flexible structure and alidade modes. The complexity of the changes to several elements of matrix **F** necessitate the reproduction of the revised version in its entirety, below.

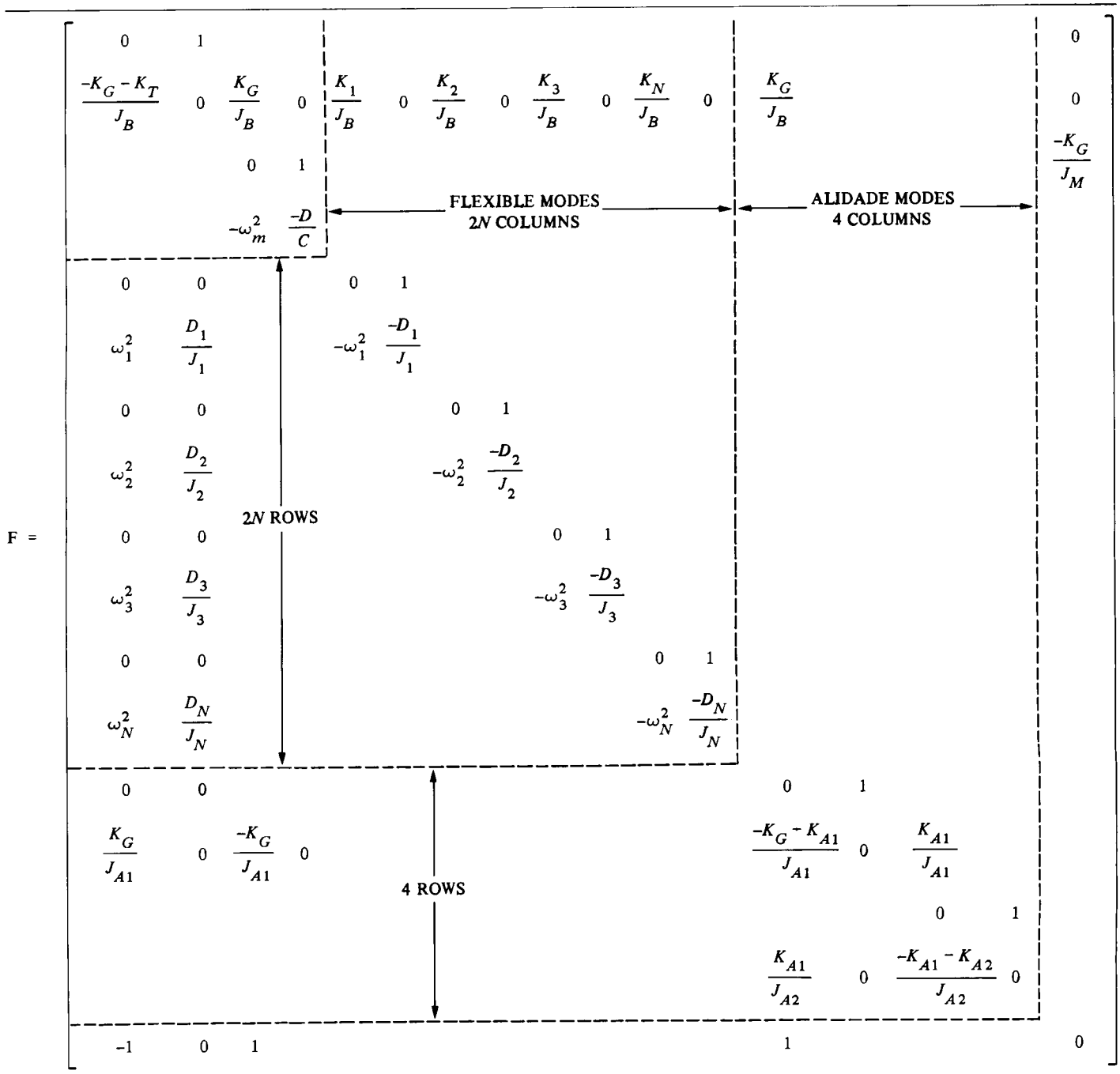
Also in Table 3 (page 255), the output vector H_{Ee} should appear:

$$H_{Ee} = [1\ 0\ 0\ 0\ \ldots\ -1\ 0\ 0\ 0\ 0]\ \text{Elevation only}$$

In the Notes section of Table 3 (page 255), the following errata were submitted:

Is	Should Be
$a1 \ldots a5$	$a_1 \ldots a_5$
$a0$	a_0
$a0 + a1 + \ldots aN = 1$	$a_0 + a_1 + \ldots a_N = 1$

Finally, in Table 4 (page 256), the term $\frac{\omega_m^2}{\nu}$ should be $\frac{\omega_m^2}{V}$.



With $K_T = \sum_1^N K_i$ and $\omega_i^2 = \frac{K_i}{J_i}$

Note: The matrix **F** is defined in a generalized form with a variable N, corresponding to the number of flexible modes (not including alidade modes) and is illustrated for the special case of $N = 4$. With the deletion of the rows and columns corresponding to the alidade, the generalized matrix structure is applicable to the azimuth axis. It should be noted that the F matrix structure is similar to a variant of the Jordan canonical form in that the damping coefficients appear along the diagonal and the squared natural frequencies appear along the subdiagonal with unit elements along the superdiagonal.

OMIT 70
END

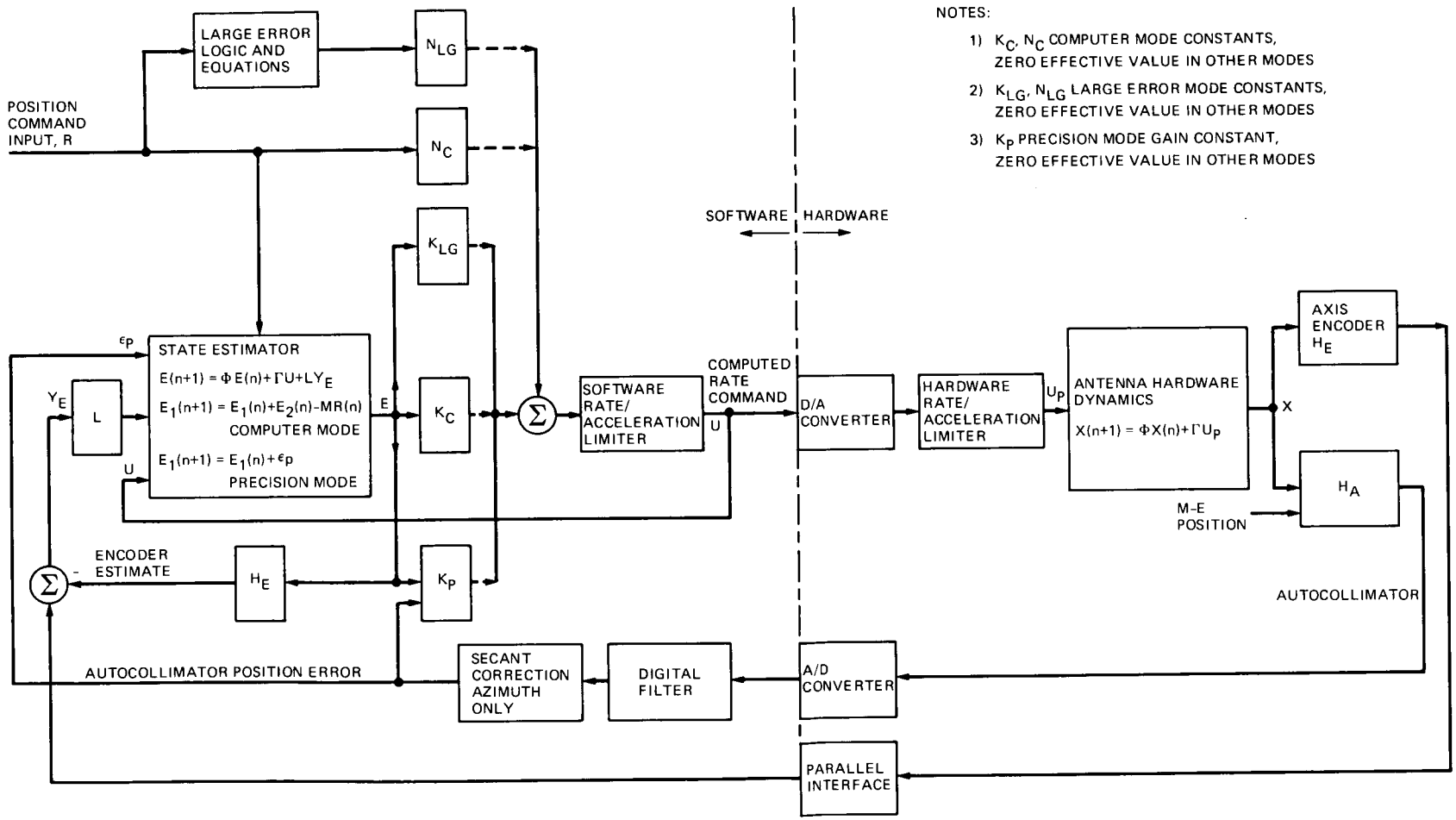
Errata

R. E. Hill (Ground Antenna and Facilities Engineering Section) has submitted the following errata to his article "A Modern Control Theory Based Algorithm for Control of the NASA/JPL 70-Meter Antenna Axis Servos" that appeared in the *Telecommunications and Data Acquisition Progress Report 42-91*, July–September 1987, November 15, 1987:

In the block diagram of Fig. 1 (page 294), a signal path from the Position Command Input to the State Estimator was omitted in error. Also, the estimator state equation for $E_1(n+1)$ for computer mode, which is printed in the State Estimator block, should be

$$E_1(n+1) = E_1(n) + E_2(n) - MR(n)$$

where for this application, M = 1. The corrected diagram is reproduced below.


NOTES:
1) K_C, N_C COMPUTER MODE CONSTANTS, ZERO EFFECTIVE VALUE IN OTHER MODES
2) K_{LG}, N_{LG} LARGE ERROR MODE CONSTANTS, ZERO EFFECTIVE VALUE IN OTHER MODES
3) K_P PRECISION MODE GAIN CONSTANT, ZERO EFFECTIVE VALUE IN OTHER MODES
LARGE ERROR LOGIC AND EQUATIONS
N_{LG}
POSITION COMMAND INPUT, R
N_C
K_{LG}
SOFTWARE
HARDWARE
ϵ_P
STATE ESTIMATOR
$E(n+1) = \Phi E(n) + \Gamma U + LY_E$
$E_1(n+1) = E_1(n) + E_2(n) - MR(n)$
COMPUTER MODE
$E_1(n+1) = E_1(n) + \epsilon_P$
PRECISION MODE
Y_E
L
U
E
K_C
SOFTWARE RATE/ ACCELERATION LIMITER
COMPUTED RATE COMMAND
U
D/A CONVERTER
HARDWARE RATE/ ACCELERATION LIMITER
U_P
ANTENNA HARDWARE DYNAMICS
$X(n+1) = \Phi X(n) + \Gamma U_P$
X
AXIS ENCODER H_E
H_A
M-E POSITION
AUTOCOLLIMATOR
ENCODER ESTIMATE
H_E
K_P
AUTOCOLLIMATOR POSITION ERROR
SECANT CORRECTION AZIMUTH ONLY
DIGITAL FILTER
A/D CONVERTER
PARALLEL INTERFACE

Author Index,[1] 1988

The Telecommunications and Data Acquisition Progress Report

42-93, January–March, May 15, 1988
42-94, April–June, August 15, 1988
42-95, July–September, November 15, 1988
42-96, October–December, February 15, 1989

Aguirre, S.

42-94 An Automatic Frequency Control Loop Using Overlapping DFTs, pp. 222–231.

Amorose, R. J.

42-93 Mark IV-85 Mission Support Planning and Future Mission Set, pp. 265–270.

Armstrong, J. W.

42-94 Gravitational Wave Searches Using the DSN, pp. 75–85.

See Nelson, S. J.

Arnold, S.

42-94 A Software Simulation Study of the Long Constraint Length VLSI Viterbi Decoder, pp. 210–221.

S. Arnold and F. Pollara

Asmar, S. W.

42-95 Two-Way Coherent Doppler Error Due to Solar Corona, pp. 28–31.

See Kinman, P. W.

Bagby, D. G.

42-93 Heat Exchanger Demonstration Expert System, pp. 177–187.

D. G. Bagby and R. A. Cormier

Ballingall, J. M.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Bathker, D. A.

42-95 DSN 70-Meter Antenna X-Band Gain, Phase, and Pointing Performance, With Particular Application for Voyager 2 Neptune Encounter, pp. 237–245.

See Slobin, S. D.

Bautista, J. J.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

J. J. Bautista, G. G. Ortiz, K. H. G. Duh, W. F. Kopp, P. Ho, P. C. Chao, M. Y. Kao, P. M. Smith, and J. M. Ballingall

Bertiger, W. I.

42-93 The Limits of Direct Satellite Tracking With the Global Positioning System (GPS), pp. 1–7.

W. I. Bertiger and T. P. Yunck

Bertiger, W. I.

42-95 Determination of GPS Orbits to Submeter Accuracy, pp. 14–27.

W. I. Bertiger, S. M. Lichten, and E. C. Katsigris

[1] In case of joint authorship, the reader is referred to the citation under the first author where all authors of the article are listed.

Bhanji, A. M.

42-95 Conceptual Design of a 1-MW CW X-Band Transmitter for Planetary Radar, pp. 97–111.

A. M. Bhanji, D. J. Hoppe, B. L. Conroy, and A. J. Freiley

Breuer, M. A.

42-96 Test Aspects of the JPL Viterbi Decoder, pp. 51–79.

Brokl, S.

42-93 Goldstone Solar System Radar Performance Analysis, pp. 302–308.

See Satorius, E.

Brown, D. H.

42-93 Advanced Receiver Tracking of Voyager 2 Near Solar Conjunction, pp. 75–82.

D. H. Brown, W. J. Hurd, V. A. Vilnrotter, and J. D. Wiggins

Brown, D. H.

42-93 Telemetry SNR Improvement Using the DSN Advanced Receiver With Results for Pioneer 10, pp. 64–74.

See Hurd, W. J.

Brown, D. H.

42-93 Spectral Estimation of Received Phase in the Presence of Amplitude Scintillation, pp. 8–17.

See Vilnrotter, V. A.

Brunzie, T. J.

42-93 An 8.4-GHz Dual Maser Front End for Parkes Reimplementation, pp. 214–228.

See Trowbridge, D. L.

Chao, P. C.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Chen, C. C.

42-93 Performance Analysis of a Noncoherently Combined Large Aperture Optical Heterodyne Receiver, pp. 131–145.

Chen, C. C.

42-93 Effect of Detector Dead Time on the Performance of Optical Direct-Detection Communication Links, pp. 146–154.

Chen, C. C.

42-94 Design of an Optical PPM Communication Link in the Presence of Component Tolerances, pp. 170–179.

Chen, C. C.

42-95 Effect of Earth Albedo Variation on the Performance of a Spatial Acquisition Subsystem Aboard a Planetary Spacecraft, pp. 202–211.

Chen, J.

42-95 Cross-Guide Coupler Modeling and Design, pp. 82–88.

Chen, J.

42-96 Microwave Time Delays for the Dual L-C-Band Feed System, pp. 126–131.

Cheng, U.

42-94 Node Synchronization of Viterbi Decoders Using State Metrics, pp. 201–209.

Cheung, K. M.

42-93 Efficient Multiplication Algorithms Over the Finite Fields $GF(q^m)$, Where $q = 3,5$, pp. 155–162.

See Truong, T. K.

Cheung, K. M.

42-94 Phobos Lander Coding System: Software and Analysis, pp. 274–286.

K. M. Cheung and F. Pollara

Cheung, K. M.

42-95 Performance of Galileo's Concatenated Codes With Nonideal Interleaving, pp. 148–152.

K. M. Cheung and S. J. Dolinar

Cheung, K. M.

42-95 Long Decoding Runs for Galileo's Convolutional Codes, pp. 143–147.

See Lahmeyer, C. R.

Christman, J. M.

42-94 Evaluation of the Characteristics of a Field Emission Cathode for Use in a Mercury Ion Trap Frequency Standard, pp. 86–92.

Clauss, R. C.

42-96 Ka-Band Study–1988, pp. 158–171.

See Layland, J. W.

Collier, J. W.

42-96 Block Diagrams of the Radar Interface Control Unit, pp. 104–116.

Collins, O.

42-95 A Long Constraint Length VLSI Viterbi Decoder for the DSN, pp. 134–142.

See Statman, J.

Collins, O.

42-96 Wiring Viterbi Decoders (Splitting deBruijn Graphs), pp. 93–103.

O. Collins, F. Pollara, S. Dolinar, and J. Statman

Conroy, B. L.

42-95 Transmitter Data Collection Using Ada, pp. 229–236.

Conroy, B. L.

42-95 Conceptual Design of a 1-MW CW X-Band Transmitter for Planetary Radar, pp. 97–111.

See Bhanji, A. M.

Cormier, R. A.

42-93 Heat Exchanger Demonstration Expert System, pp. 177–187.

See Bagby, D. G.

Cormier, R.

42-94 Heat Exchanger Expert System Logic, pp. 232–244.

Cormier, R.

42-96 Design and Test of a 2.25-MW Transformer Rectifier Assembly, pp. 1–13.

R. Cormier and J. Daeges

Cowles, K.

42-95 Performance of Efficient Q-Switched Diode-Laser-Pumped Nd:YAG and Ho:YLF Lasers for Space Applications, pp. 168–173.

See Marshall, W. K.

Daeges, J.

42-96 Design and Test of a 2.25-MW Transformer Rectifier Assembly, pp. 1–13.

See Cormier, R.

de Groot, N. F.

42-93 New CCIR Report on SETI, pp. 280–291.

DeVore, C. W.

42-95 Shutters and Slats for the Integral Sunshade of an Optical Reception Antenna, pp. 196–201.

See Kerr, E. L.

Densmore, A. C.

42-93 A Digitally Implemented Phase-Locked Loop Detection Scheme for Analysis of the Phase and Power Stability of a Calibration Tone, pp. 207–213.

Divsalar, D.

42-96 The Use of Interleaving for Reducing Radio Loss in Convolutionally Coded Systems, pp. 21–39.

D. Divsalar, M. K. Simon, and J. H. Yuen

Doerksen, I.

42-93 Baseband Assembly Analog-to-Digital Converter Board, pp. 257–264.

I. Doerksen and L. Howard

Dolinar, S.

42-93 A New Code for Galileo, pp. 83–96.

Dolinar, S. J.

42-95 VLA Telemetry Performance With Concatenated Coding for Voyager at Neptune, pp. 112–133.

Dolinar, S. J.

42-95 Performance of Galileo's Concatenated Codes With Nonideal Interleaving, pp. 148–152.

See Cheung, K. M.

Dolinar, S.

42-96 Wiring Viterbi Decoders (Splitting deBruijn Graphs), pp. 93–103.

See Collins, O.

Duh, K. H.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Ellis, J.

42-93 Determination of the Venus Flyby Orbits of the Soviet Vega Probes Using VLBI Techniques, pp. 271–279.

J. Ellis and T. P. McElrath

Esquivel, M.

42-94 X/X/Ka-Band Prime Focus Feed Antenna for the Mars Observer Beacon Spacecraft, pp. 103–109.

See Stanton, P.

Fanelli, N. A.

42-94 Summary of DSN Reimbursable Launch Support, pp. 301–305.

N. A. Fanelli and M. E. Wyatt

Franco, M. M.

42-94 Dual Passband Dichroic Plate for X-Band, pp. 110–134.

See Otoshi, T. Y.

Freiley, A. J.

42-94 Simultaneous S- and X-Band Uplink-Downlink Performance at DSS 13, pp. 93–102.

Freiley, A. J.

42-95 Conceptual Design of a 1-MW CW X-Band Transmitter for Planetary Radar, pp. 97–111.

See Bhanji, A. M.

Freiley, A. J.

42-96 RF Performance Measurement of the DSS-14 70-Meter Antenna at C-Band/L-Band, pp. 117–125.

See Gatti, M. S.

Gary, B. L.

42-94 Spain 31-GHz Observations of Sky Brightness Temperatures, pp. 42–60.

Gary, B. L.

42-94 Australia 31-GHz Brightness Temperature Exceedance Statistics, pp. 61–74.

Garyantes, M. F.

42-93 A Wideband, High-Resolution Spectrum Analyzer, pp. 188–198.

See Quirk, M. P.

Gatti, M. S.

42-96 RF Performance Measurement of the DSS-14 70-Meter Antenna at C-Band/L-Band, pp. 117–125.

M. S. Gatti, A. J. Freiley, and D. Girdner

Girdner, D.

42-96 RF Performance Measurement of the DSS-14 70-Meter Antenna at C-Band/L-Band, pp. 117–125.

See Gatti, M. S.

Gosline, R. M.

42-93 DSS 13 Microprocessor Antenna Controller, pp. 163–176.

Gresham, L. L.

42-93 The Feasibility of the Disturbance Accommodating Controller for Precision Antenna Pointing, pp. 27–44.

L. L. Gresham, F. L. Lansing, and C. N. Guiar

Grimm, M. J.

42-93 A Wideband, High-Resolution Spectrum Analyzer, pp. 188–198.

See Quirk, M. P.

Guiar, C. N.

42-93 The Feasibility of the Disturbance Accommodating Controller for Precision Antenna Pointing, pp. 27–44.

See Gresham, L. L.

Guiar, C. N.

42-93 DSS 14 Antenna Calibrations for GSSR/VLA Saturn Radar Experiments, pp. 309–337.

C. N. Guiar, R. L. Riggs, R. Stevens, and M. Wert

Gulkis, S.

42-96 Radio Frequency Interference Survey Over the 1.0–10.4 GHz Frequency Range at the Goldstone-Venus Development Station, pp. 179–188.

S. Gulkis, E. T. Olsen, M. J. Klein, and E. B. Jackson

Hemmati, H.

42-95 Performance of Efficient Q-Switched Diode-Laser-Pumped Nd:YAG and Ho:YLF Lasers for Space Applications, pp. 168–173.

See Marshall, W. K.

Hill, R. E.

42-95 Dynamic Models for Simulation of the 70-M Antenna Axis Servos, pp. 32–50.

Hill, R. E.

42-95 A New Algorithm for Modeling Friction in Dynamic Mechanical Systems, pp. 51–57.

Hinedi, S.

42-95 An Extended Kalman Filter Based Automatic Frequency Control Loop, pp. 219–228.

Ho, P.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Holmes, J. K.

42-96 A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes, pp. 49–58.

See Truong, T. K.

Hoppe, D.

42-93 X-Band Resonant Ring Operation at 450 kW, pp. 18–26.

D. Hoppe and R. Perez

Hoppe, D. J.

42-95 Modal Analysis Applied to Circular, Rectangular, and Coaxial Waveguides, pp. 89–96.

Hoppe, D. J.

42-95 Conceptual Design of a 1-MW CW X-Band Transmitter for Planetary Radar, pp. 97–111.

See Bhanji, A. M.

Horttor, R. L.

42-96 Ka-Band Study—1988, pp. 158–171.

See Layland, J. W.

Howard, L.

42-93 Baseband Assembly Analog-to-Digital Converter Board, pp. 257–264.

See Doerksen, I.

Hsu, I. S.

42-93 Efficient Multiplication Algorithms Over the Finite Fields $GF(q^m)$, where $q = 3,5$, pp. 155–162.

See Truong, T. K.

Hsu, I. S.

42-96 On Testing VLSI Chips for the Big Viterbi Decoder, pp. 80–92.

Hsu, I. S.

42-96 A New VLSI Architecture for a Single-Chip-Type Reed-Solomon Decoder, pp. 40–48.

I. S. Hsu and T. K. Truong

Hurd, W. J.

42-93 Telemetry SNR Improvement Using the DSN Advanced Receiver With Results for Pioneer 10, pp. 64–74.

W. J. Hurd, D. H. Brown, V. A. Vilnrotter, and J. D. Wiggins

Hurd, W. J.

42-93 Advanced Receiver Tracking of Voyager 2 Near Solar Conjunction, pp. 75–82.

See Brown, D. H.

Hurd, W. J.

42-93 Digital Carrier Demodulation for the DSN Advanced Receiver, pp. 45–63.

See Sadr, R.

Hurd, W. J.

42-93 Spectral Estimation of Received Phase in the Presence of Amplitude Scintillation, pp. 8–17.

See Vilnrotter, V. A.

Jackson, E. B.

42-96 Radio Frequency Interference Survey Over the 1.0–10.4 GHz Frequency Range at the Goldstone-Venus Development Station, pp. 179–188.

See Gulkis, S.

Jenkins, B.

42-93 An 8.4-GHz Dual Maser Front End for Parkes Reimplementation, pp. 214–228.

See Trowbridge, D. L.

Kao, M. Y.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Katsigris, E. C.

42-95 Determination of GPS Orbits to Submeter Accuracy, pp. 14–27.

See Bertiger, W. I.

Kerr, E. L.

42-93 Strawman Optical Reception Development Antenna (SORDA), pp. 97–110.

Kerr, E. L.

42-95 An Integral Sunshade for Optical Reception Antennas, pp. 180–195.

Kerr, E. L.

42-95 Shutters and Slats for the Integral Sunshade of an Optical Reception Antenna, pp. 196–201.

E. L. Kerr and C. W. DeVore

Kinman, P. W.

42-95 Two-Way Coherent Doppler Error Due to Solar Corona, pp. 28–31.

P. W. Kinman and S. W. Asmar

Klein, M. J.

42-96 Radio Frequency Interference Survey Over the 1.0–10.4 GHz Frequency Range at the Goldstone-Venus Development Station, pp. 179–188.

See Gulkis, S.

Kopp, W. F.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Lahmeyer, C. R.

42-95 Long Decoding Runs for Galileo's Convolutional Codes, pp. 143–147.

C. R. Lahmeyer and K. M. Cheung

Lakshminarayana, M.

42-93 An Electronically Tuned, Stable 8415-MHz Dielectric Resonator FET Oscillator for Space Applications, pp. 292–301.

Lansing, F. L.

42-93 The Feasibility of the Disturbance Accommodating Controller for Precision Antenna Pointing, pp. 27–44.

See Gresham, L. L.

Layland, J. W.

42-96 Ka-Band Study–1988, pp. 158–171.

J. W. Layland, R. L. Horttor, R. C. Clauss, J. H. Wilcher, R. J. Wallace, and D. J. Mudgway

Legerton, V. N.

42-94 PSA: A Program to Streamline Orbit Determination for Launch Support Operations, pp. 28–41.

V. N. Legerton and N. A. Mottinger

Lichten, S. M.

42-95 Determination of GPS Orbits to Submeter Accuracy, pp. 14–27.

See Bertiger, W. I.

Liewer, K. M.

42-93 DSN Very Long Baseline Interferometry System Mark IV-88, pp. 239–246.

Loreman, J.

42-93 2.3-GHz Low-Noise Cryo-FET Amplifier, pp. 199–206.

Loreman, J. R.

42-93 An 8.4-GHz Dual Maser Front End for Parkes Reimplementation, pp. 214–228.

See Trowbridge, D. L.

Lyons, J. R.

42-95 Theoretical Comparison of Maser Materials for a 32-GHz Maser Amplifier, pp. 58–70.

Malla, R. P.

42-95 Deriving a Geocentric Reference Frame for Satellite Positioning and Navigation, pp. 1–13.

R. P. Malla and S. C. Wu

Marshall, W. K.

42-95 Performance of Efficient Q-Switched Diode-Laser-Pumped Nd:YAG and Ho:YLF Lasers for Space Applications, pp. 168–173.

W. K. Marshall, K. Cowles, and H. Hemmati

McEliece, R. J.

42-95 The Decoding of Reed-Solomon Codes, pp. 153–167.

McElrath, T. P.

42-93 Determination of the Venus Flyby Orbits of the Soviet Vega Probes Using VLBI Techniques, pp. 271–279.

See Ellis, J.

Mileant, A.

42-95 Pointing a Ground Antenna at a Spinning Spacecraft Using Conscan—Simulation Results, pp. 246–260.

A. Mileant and T. Peng

Mottinger, N. A.

42-94 PSA: A Program to Streamline Orbit Determination for Launch Support Operations, pp. 28–41.

See Legerton, V. N.

Mudgway, D. J.

42-96 Ka-Band Study—1988, pp. 158–171.

See Layland, J. W.

Muellerschoen, R. J.

42-94 Storage and Computationally Efficient Permutations of Factorized Covariance and Square-Root Information Arrays, pp. 245–256.

Mysoor, N.

42-96 A Low-Loss Linear Analog Phase Modulator for 8415 MHz Transponder Application, pp. 172–178.

Neff, D.

42-94 A 32-GHz Reflected-Wave Maser Amplifier With Wide Instantaneous Bandwidth, pp. 145–162.

See Shell, J.

Nelson, S. J.

42-94 Gravitational Wave Searches Using the DSN, pp. 75–85.

S. J. Nelson and J. W. Armstrong

Nguyen, T. M.

42-93 The Behavior of a Costas Loop in the Presence of Space Telemetry Signals, pp. 229–238.

Olsen, E. T.

42-96 Radio Frequency Interference Survey Over the 1.0–10.4 GHz Frequency Range at the Goldstone-Venus Development Station, pp. 179–188.

See Gulkis, S.

Ortiz, G. G.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Otoshi, T. Y.

42-94 Dual Passband Dichroic Plate for X-Band, pp. 110–134.

T. Y. Otoshi and M. M. Franco

Peng, T. K.

42-93 X-Band Noise Temperature Near the Sun at a 34-Meter High Efficiency Antenna, pp. 247–256.

See Rebold, T. A.

Peng, T.

42-95 Pointing a Ground Antenna at a Spinning Spacecraft Using Conscan—Simulation Results, pp. 246–260.

See Mileant, A.

Perez, R.

42-93 X-Band Resonant Ring Operation at 450 kW, pp. 18–26.

See D. Hoppe

Pollara, F.

42-94 A Software Simulation Study of the Long Constraint Length VLSI Viterbi Decoder, pp. 210–221.

See Arnold, S.

Pollara, F.

42-94 Phobos Lander Coding System: Software and Analysis, pp. 274–286.

See Cheung, K. M.

Pollara, F.

42-95 A Long Constraint Length VLSI Viterbi Decoder for the DSN, pp. 134–142.

See Statman, J.

Pollara, F.

42-96 Wiring Viterbi Decoders (Splitting deBruijn Graphs), pp. 93–103.

See Collins, O.

Quirk, M. P.

42-93 A Wideband, High-Resolution Spectrum Analyzer, pp. 188–198.

M. P. Quirk, H. C. Wilck, M. F. Garyantes, and M. J. Grimm

Rayman, M. D.

42-95 Calculations of Laser Cavity Dumping for Optical Communications, pp. 174–179.

See Robinson, D. L.

Rebold, T. A.

42-93 X-Band Noise Temperature Near the Sun at a 34-Meter High Efficiency Antenna, pp. 247–256.

T. A. Rebold, T. K. Peng, and S. D. Slobin

Reed, I. S.

42-93 Efficient Multiplication Algorithms Over the Finite Fields $GF(q^m)$, Where $q = 3,5$, pp. 155–162.

See Truong, T. K.

Reed, I. S.

42-96 A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes, pp. 49–58.

See Truong, T. K.

Reilly, H.

42-94 X/X/Ka-Band Prime Focus Feed Antenna for the Mars Observer Beacon Spacecraft, pp. 103–109.

See Stanton, P.

Renzetti, N. A.

42-94 Relative Planetary Radar Sensitivities: Arecibo and Goldstone, pp. 287–293.

N. A. Renzetti, T. W. Thompson, and M. A. Slade

Riggs, R. L.

42-93 DSS 14 Antenna Calibrations for GSSR/VLA Saturn Radar Experiments, pp. 309–337.

See Guiar, C. N.

Robinson, D. L.

42-95 Calculations of Laser Cavity Dumping for Optical Communications, pp. 174–179.

D. L. Robinson and M. D. Rayman

Rochblatt, D. J.

42-96 Systems Analysis for DSN Microwave Antenna Holography, pp. 132–157.

Sadr, R.

42-93 Digital Carrier Demodulation for the DSN Advanced Receiver, pp. 45–63.

R. Sadr and W. J. Hurd

Sadr, R.

42-96 On Sampling Band-Pass Signals, pp. 14–20.

R. Sadr and M. Shahshahani

Satorius, E.

42-93 Goldstone Solar System Radar Performance Analysis, pp. 302–308.

E. Satorius and S. Brokl

Schumacher, L. L.

42-94 Antenna Pointing Compensation Based on Precision Optical Measurement Techniques, pp. 135–144.

L. L. Schumacher and H. C. Vivian

Schumaker, B. L.

42-93 Apparent Brightness of Stars and Lasers, pp. 111–130.

Shahshahani, M.

42-96 On Sampling Band-Pass Signals, pp. 14–20.

See Sadr, R.

Shaik, K. S.

42-94 Atmospheric Propagation Effects Relevant to Optical Communications, pp. 180–200.

Shaik, K. S.

42–95 A Preliminary Weather Model for Optical Communications Through the Atmosphere, pp. 212–218.

Shell, J.

42-94 A 32-GHz Reflected-Wave Maser Amplifier With Wide Instantaneous Bandwidth, pp. 145–162.

J. Shell and D. Neff

Simon, M. K.

42-96 The Use of Interleaving for Reducing Radio Loss in Convolutionally Coded Systems, pp. 21–39.

See Divsalar, D.

Slade, M. A.

42–94 Relative Planetary Radar Sensitivities: Arecibo and Goldstone, pp. 287–293.

See Renzetti, N. A.

Slobin, S. D.

42–93 X-Band Noise Temperature Near the Sun at a 34-Meter High Efficiency Antenna, pp. 247–256.

See Rebold, T. A.

Slobin, S. D.

42-95 DSN 70-Meter Antenna X-Band Gain, Phase, and Pointing Performance, With Particular Application for Voyager 2 Neptune Encounter pp. 237–245.

S. D. Slobin and D. A. Bathker

Smith, P. M.

42-95 32-GHz Cryogenically Cooled HEMT Low-Noise Amplifiers, pp. 71–81.

See Bautista, J. J.

Stanton, P.

42-94 X/X/Ka-Band Prime Focus Feed Antenna for the Mars Observer Beacon Spacecraft, pp. 103–109.

P. Stanton, H. Reilly, and M. Esquivel

Statman, J.

42-95 A Long Constraint Length VLSI Viterbi Decoder for the DSN, pp. 134-142.

J. Statman, G. Zimmerman, F. Pollara, and O. Collins

Statman, J.

42-96 Wiring Viterbi Decoders (Splitting deBruijn Graphs), pp. 93–103.

See Collins, O.

Stevens, R.

42-93 DSS 14 Antenna Calibrations for GSSR/VLA Saturn Radar Experiments, pp. 309–337.

See Guiar, C. N.

Tanida, L.

42-94 An 8.4-GHz Cryogenically Cooled HEMT Amplifier for DSS 13, pp. 163–169.

Thompson, T. W.

42-94 Relative Planetary Radar Sensitivities: Arecibo and Goldstone, pp. 287–293.

See Renzetti, N. A.

Trowbridge, D. L.

42-93 An 8.4-GHz Dual Maser Front End for Parkes Reimplementation, pp. 214–228.

D. L. Trowbridge, J. R. Loreman, T. J. Brunzie and B. Jenkins

Truehaft, R. N.

42-94 Deep Space Tracking in Local Reference Frames, pp. 1–15.

Truong, T. K.

42-93 Efficient Multiplication Algorithms Over the Finite Fields $GF(q^m)$, Where $q = 3,5$, pp. 155–162.

T. K. Truong, I. S. Hsu, K. M. Cheung, and I. S. Reed.

Truong, T. K.

42-96 A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes, pp. 49–58.

T. K. Truong, J. K. Holmes, I. S. Reed, and X. Yin.

Truong, T. K.

42-96 A New VLSI Architecture for a Single-Chip-Type Reed-Solomon Decoder, pp. 40–48.

See Hsu, I. S.

Ulvestad, J. S.

42-94 Phasing the Antennas of the Very Large Array for Reception of Telemetry from Voyager 2 at Neptune Encounter, pp. 257–273.

Vilnrotter, V. A.

42-93 Spectral Estimation of Received Phase in the Presence of Amplitude Scintillation, pp. 8–17.

V. A. Vilnrotter, D. H. Brown, and W. J. Hurd

Vilnrotter, V. A.

42-93 Advanced Receiver Tracking of Voyager 2 Near Solar Conjunction, pp. 75–82.

See Brown, D. H.

Vilnrotter, V. A.

42-93 Telemetry SNR Improvement Using the DSN Advanced Receiver With Results for Pioneer 10, pp. 64–74.

See Hurd, W. J.

Vivian, H. C.

42-94 Antenna Pointing Compensation Based on Precision Optical Measurement Techniques, pp. 135–144.

See Schumacher, L. L.

Wallace, R. J.

42-96 Ka-Band Study – 1988, pp. 158–171.

See Layland, J. W.

Wert, M.

42-93 DSS 14 Antenna Calibrations for GSSR/VLA Saturn Radar Experiments, pp. 309–337.

See Guiar, C. N.

Wiggins, J. D.

42-93 Advanced Receiver Tracking of Voyager 2 Near Solar Conjunction, pp. 75–82.

See Brown, D. H.

Wiggins, J. D.

42-93 Telemetry SNR Improvement Using the DSN Advanced Receiver With Results for Pioneer 10, pp. 64–74.

See Hurd, W. J.

Wilcher, J. H.

42-96 Ka-Band Study – 1988, pp. 158–171.

See Layland, J. W.

Wilck, H. C.

42-93 A Wideband, High-Resolution Spectrum Analyzer, pp. 188–198.

See Quirk, M. P.

Williams, B. G.

42-94 Precise Orbit Determination for NASA's Earth Observing System Using GPS, pp. 16–27.

Withington, J.

42-94 DSN 64-Meter Antenna L-Band (1668 MHz) Microwave System Performance Overview, pp. 294–300.

Wu, S. C.

42-95 Deriving a Geocentric Reference Frame for Satellite Positioning and Navigation, pp. 1–13.

See Malla, R. P.

Wyatt, M. E.

42-94 Summary of DSN Reimbursable Launch Support, pp. 301–305.

See Fanelli, N. A.

Yin, X.

42-96 A Simplified Procedure for Decoding the (23,12) and (24,12) Golay Codes, pp. 49–58.

See Truong, T. K.

Yuen, J. H.

42-96 The Use of Interleaving for Reducing Radio Loss in Convolutionally Coded Systems, pp. 21–39.

See Divsalar, D.

Yunck, T. P.

42-93 The Limits of Direct Satellite Tracking With the Global Positioning System (GPS), pp. 1–7.

See Bertiger, W. I.

Zimmerman, G.

42-95 A Long Constraint Length VLSI Viterbi Decoder for the DSN, pp. 134–142.

See Statman, J.